INVESTIGATIONS ON PERFORMANCE

EVALUATION OF CMOS VLSI

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By

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DEEMED UNIVERSITY)

SALEM, TAMILNADU, INDIA

MARCH 2015
VINAYAKA MISSIONS UNIVERSITY
SALEM

DECLARATION

I, T.Sheela, declare that the thesis entitled INVESTIGATIONS ON PERFORMANCE EVALUATION OF CMOS VLSI submitted by me for the Degree of Doctor of Philosophy is the record of work carried out by me during the period from 2009 to 2015 under the guidance of Dr. A. Nagappan, and has not formed the basis for the award of any degree, diploma, associate-ship, fellowship, titles in this or any other University or other similar institutions of higher learning.

Place: Salem
Date: Signature of the Candidate
I, Dr. A. Nagappan, certify that the thesis entitled **INVESTIGATIONS ON PERFORMANCE EVALUATION OF CMOS VLSI** submitted for the Degree of Doctor of Philosophy by Ms. T. Sheela, is the record of research work carried out by him during the period **from 2009 to 2015** under my guidance and supervision and that this work has not formed the basis for the award of any degree, diploma, associate-ship, fellowship or other titles in this University or any other University or Institution of higher learning.

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ABSTRACT

The progression in very large scale integration, billions of transistors and components can be placed on a single semiconductor chip for implementation of complex circuitry. The growth in recent technology is towards miniaturization of semiconductor devices, which have several noticeable hindrances in heat dissipation, power utility, chip area and efficiency of the devices. As the technology advances more into deep submicron level, feature sizes, power dissipation due to leakage current are increasing at an alarming rate. Numerous projections show that leakage power will develop into analogous to dynamic power dissipation in coming years; however dynamic power is also increasing and still dominates. The optimal solution for solving these hindrances is to analyze the performance of Very Large Scale Integration (VLSI) circuit designed using different Complementary Metal Oxide Semiconductor (CMOS) technologies.

CMOS design of Linear Feedback Shift Register (LFSR) is taken for the performance evaluation, owing to its prevalent usage in a variety of applications like circuit testing, digital broadcasting, Built-in self-test (BIST), cryptography, pseudo-noise sequence generator, etc. Despite the fact that a number of architectures for the VLSI implementation of LFSR
are reported, it is observed that some of these architectures have low performance, low throughput, less area efficient and high cost upon implementation. Counters such as Binary and Gray also suffer problems in power consumption, delay, glitches and speed because they are implemented with techniques which have above drawbacks.

The existing design not only produces glitches which increase power consumption however there is design complexity leading to propagation delays, hence there is degradation in speed & performance of system. Therefore a reliable architecture for LFSR with high performance, low-power and cost effective design is needed. The previous research works are austerely focused on area and cost of efficient architectural design with petite focus on performance and power. This research work focuses on performance evaluation of the design.

In this research a D flip-flop known as kernel for LFSR, is designed using CMOS VLSI logics like pass transistor and dynamic CMOS logic. The layout diagrams and synthesis reports were generated for the design. The synthesis report showed that the dynamic logic uses minimum number of transistors and consequently has better performances with minimum power consumption and chip area, when compared with the D flip-flop designed using pass transistor logic. The performances of the D flip-flop
designed using dynamic logic are compared with the D flip-flop designed using other logics. Based on the comparative study it is identified that D flip-flop designed using dynamic logic utilizes minimum power, produces minimum delay and occupies less chip area. Therefore the dynamic logic is identified as efficient and it is used in the design of entire LFSR counter architecture.

Despite several advantages in dynamic logic, there are several drawbacks in handling the slender charge leakages in the CMOS circuits as results of unwanted conduction paths like subthreshold and reverse PN-junction currents, and high clock frequency requirement to induce pre-transition states. The drawbacks which shrink the performance of CMOS design of LFSR architecture are overcome by use of an efficient multi-threshold voltage level converter in the CMOS architecture.

The proposed level converter employs a multi-threshold (V_{TH}) CMOS technology with a high threshold voltage pull-up transistors network which is directly driven by the low swing signals. The converter does not have a feedback path between the input and output, hence eliminates the static dc current dissipation. The proposed converter is compared with several multi-threshold voltage level converter circuits for low and high threshold voltages. Based upon the comparative analyses result, the proposed
converter is identified as the efficient level converter with high processing speed and low power utilization.

The proposed level converter offers significant power saving and speed enhancement for CMOS VLSI design of LFSR counter architecture, by eliminating the static dc current and charge leakage existing in the CMOS circuits. Therefore the combination of dynamic logic with level converter is considered as novel with reasonable area and time complexity overheads, possessing maximum efficiency and better reliability.
ACKNOWLEDGEMENT

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(T.SHEELA)
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<td>AFSR</td>
<td>Algebraic Feedback Shift Register</td>
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<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
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<td>BICMOS</td>
<td>Bipolar Complementary Metal Oxide Semiconductor</td>
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<tr>
<td>BIST</td>
<td>Built-In Self-Test</td>
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<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
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<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
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<td>CLK</td>
<td>Clock</td>
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<tr>
<td>DSM</td>
<td>Deep Sub Micron Technology</td>
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<td>FCSR</td>
<td>Feedback with Carry Shift Register</td>
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<td>GIDL</td>
<td>Gate Induced Drain Leakage</td>
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<td>GND</td>
<td>Ground</td>
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<td>HSPICE</td>
<td>H-Simulation Program with Integrated Circuit Emphasis</td>
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<tr>
<td>IBM</td>
<td>International Business Machine</td>
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<td>IC</td>
<td>Integrated Circuit</td>
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<td>ISE</td>
<td>Integrated Software Environment</td>
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<td>LFSR</td>
<td>Linear Feedback Shift Register</td>
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<td>Low Power Linear Feedback Shift Register</td>
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<td>Term</td>
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<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
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<td>MTCMOS</td>
<td>Multi-threshold CMOS</td>
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<td>MULTI-$V_{TH}$</td>
<td>Multi-threshold Voltage</td>
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<td>NMOS</td>
<td>N-type Metal Oxide Semiconductor</td>
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<td>OR gate</td>
<td>Logic gate</td>
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<td>$P_d$</td>
<td>Dynamic Power dissipation</td>
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<td>PDP</td>
<td>Power Delay Product</td>
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<td>PMOS</td>
<td>P-type Metal Oxide Semiconductor</td>
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<tr>
<td>$P_s$</td>
<td>Static Power dissipation</td>
</tr>
<tr>
<td>$P_{sc}$</td>
<td>Short Circuit Power dissipation</td>
</tr>
<tr>
<td>SoC</td>
<td>Systems on Chip</td>
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<tr>
<td>$V_{DD}$</td>
<td>Drain to drain Supply Voltage</td>
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<td>$V_{DDH}$</td>
<td>High level Supply Voltage</td>
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<tr>
<td>$V_{DDL}$</td>
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<tr>
<td>VHDL</td>
<td>Very High speed Hardware Description Language</td>
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<td>VLSI</td>
<td>Very Large Scale Integration</td>
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<td>VSS</td>
<td>Ground voltage</td>
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$V_{\text{throll-off}}$ & Threshold Voltage roll off \\
XOR & Exclusive OR gate
CHAPTER 1

INTRODUCTION

With advancements in large scale integration, millions of transistors can be placed on a single chip for implementation of complex circuitry. As a result of placing so many transistors in such a small space, major problems of heat dissipation and power consumption have come into the picture. The optimal solution for solving these problems is to analyze the performance of VLSI circuit designed using different CMOS technologies. A CMOS design of Linear Feedback Shift Register (LFSR) counter [11, 24, 59] is taken for the performance evaluation. LFSR is used in a variety of applications such as Built-in self-test (BIST), cryptography [77], error-correction code and in field of communication for generating pseudo-noise sequences and moreover they have a low-cost realization in hardware.

A number of architectures for the VLSI implementation of LFSR are reported. It can be observed that some of these architectures are of low performance and some provide low throughput. Further, many of the architectures are not area efficient and can result in higher cost when implemented in silicon. Counters such as Binary, Gray suffer problem of power consumption, glitches, speed, and delay because they are implemented with techniques which have above drawbacks.
The existing design not only produces glitches which increase power consumption however there is design complexity leading to propagation delays [6], hence there is degradation in speed & performance of system.

As technology moves into deep submicron [70, 71] feature sizes, power dissipation due to leakage current is increasing at an alarming rate. Projections show that leakage power will become comparable to dynamic power dissipation in the next few years; however dynamic power is also increasing and still dominates. Supply voltage has not been scaled aggressively enough to keep power per unit area constant over technology generations, which exacerbates problems in growth of die area. One of the best techniques to reduce the power consumption is scaling the supply voltage $V_{DD}$. In order to maintain generational speed enhancement, the device threshold voltage $V_{th}$ must also scale down with $V_{DD}$.

This work consider the effectiveness of the techniques of multiple threshold voltages [7, 8, 9], multiple supply voltages and sizing the combination of these techniques on both active and leakage power reduction. Level conversion penalties were considered with dual-$V_{DD}$ design. Level converters for converting voltage levels from lower voltage to higher voltage levels and its applications were analyzed.
Minimization of dynamic and static power through joint assignment of threshold voltages, sizing optimization and algorithm for minimizing standby power in deep submicron dual-$V_{th}$ circuits were analyzed. Reduction in delay between CMOS circuits by maximizing the features of wires and changing the device parameters design methodologies, for low power and high speed were discussed. Low power design techniques using clustered voltage scaling and variable supply voltage scheme, to assign multiple threshold voltages in variety of applications were analyzed.

1.1 LINEAR FEEDBACK SHIFT REGISTER (LFSR)

LFSR [52] is a shift register whose input bit is a linear function of its previous state. Some of the outputs are combined in exclusive-OR configuration to form a feedback mechanism and fed as input to any one of the flip flops. In general the register mainly includes negative edge triggered D flip-flop, and has a finite number of possible states and repeatable cycle, so as to provide a well-defined feedback function to produce a sequence of bits that are random in nature and may have a very long repeatable cycle.

1.1.1 Properties of LFSR

LFSR encloses several properties including size, length, speed, etc.
1.1.1.1 Maximal Length

As the LFSR uses cyclic binary states, use of simple XOR operation upon taping particular bit positions and shifting operation provides uniform serial computation. These states are useful in digital electronics, for testing hardware in random manner, noise generation and scramblers. Maximum length of the register is decided by its number of tap positions.

For instant, consider a 3-bit LFSR having tap positions in second and third bits generating a pattern \{001,010,011,100,101,110,111\}. The tap positions declare the length of the register, therefore the maximal length of the register is two and three. By analyzing the patterns it is found that each of the columns is rotatable and used to predict pattern for the next state. As the patterns are predictable, this type of register is not used in commercial applications and in cryptographic applications. Non-maximal length LFSR are used for random pattern generation and used in commercial applications and in cryptographic applications.

1.1.1.2 Randomness (primitive polynomials)

Each LFSR obeys 15 of 25 standard statistical tests. Consecutive numbers have a shift register relation (particularly external). Columns are identical but displaced. No number is repeated until the complete
sequence is done. Uses only a few (1 to 3) XOR gates, and D flip-flops. Internal circuit is very fast. Max delay = (1 XOR delay) + (1 D ff delay). Primitive polynomials have 2N-1 sequential states. The all zero state is always isolated. If LFSR is reset at the start, it locks up in the all zero state.

1.1.1.3 Size

A LFSR takes less area than any other common counter except a ripple counter. The ripple counter is not synchronous and much harder to interface reliably.

1.1.1.4 Speed

A LFSR is faster than any other common counters except the Mobius counter. It is used in counting applications also. It does not count in binary. It counts modulo 2N-1, a binary counter counts modulo 2N.

1.1.2 Classification of LFSR

The LFSR is classified into external feedback type and internal feedback type based on its tapping positions.

1.1.2.1 External feedback LFSR (Fibonacci LFSR)

This LFSR has two or many XOR gates that are sequentially connected with the output bit and then fed back as input to the register
to produce output stream. It has cycles through all possible $2^n - 1$ states within the shift register except the state where all bits are zero), unless it contains all zeros, in which case it will never change. It utilizes finite field arithmetic as a polynomial mod 2, with 1's and 0's as the polynomial coefficients. This is called the feedback polynomial or reciprocal characteristic polynomial. For example, if the taps are at the 14th, 13th and 9th bits (as shown), the feedback polynomial is

$$x^{14} + x^{13} + x^9 + 1 \text{ ------- (1)}$$

The '1' in the polynomial expression does not correspond to a tap and it denotes the input to the first bit (i.e. $x_0$, which is equivalent to 1). The powers of the terms represent the tapped bits, counting from the left. The first and last bits are always connected as an input and output tap respectively, with a condition that the number of taps should be even.

Figure 1.1 Block diagram of external feedback LFSR
The figure 1.1 shows the external feedback LFSR block diagram. The register uses four delay flip flops. The output of flip flops is randomly connected to XOR gates and is again fed back as input to the register. From the figure it is understood that one or more outputs of the flip flops may XOR’d depending on the requirements. It is also understood that all the clock inputs are assigned with synchronous clock signal. As the XOR operation is made at the output side of the logic it is called as external feedback LFSR.

1.1.2.2 Internal feedback LFSR (Galois LFSR)

A French mathematician Évariste Galois found a polynomial series called Galois field, a LFSR using this Galois configuration is known as Galois LFSR or modular or internal XORs or one-to-many LFSR. In the Galois configuration, when the system is clocked, bits that are not tapped however it is shifted one position to the right in unchanged manner. The taps are XOR’d with the output bit before they are stored in the next position. The new output bit is the next input bit. The effect of this is that when the output bit is zero all the bits in the register shift to the right unchanged, and the input bit becomes zero. When the output bit is one, the bits in the tap positions all flip and then the entire register is shifted to the right and the input bit becomes 1.

\[ x^{16} + x^{14} + x^9 + 1 \]
The equation shows a 16-bit Galois LFSR pattern. The register numbers in the pattern correspond to the same primitive polynomial as the Fibonacci example but are counted in reverse to the shifting direction. This register also cycles through the maximal number of 65535 states excluding the all-zeroes state. To generate the same output stream, the order of the taps is the counterpart of the order for the conventional LFSR; otherwise the stream will be in reverse. Note that the internal state of the LFSR is not necessarily the same. As Galois LFSRs do not join every tap to produce the new input, propagation times are reduced and thereby increasing the speed of execution.

Figure 1.2 Block diagram Internal Feedback LFSR

The figure 1.2 shows the internal feedback LFSR block diagram. The register includes four delay flip flops and few XOR gates. The specific flip flop output is connected to XOR gates and it is again
fed back as input to the register. XOR operations are applied to two or more flip flops depending on the sequence length. The clock input of each of the flip flops are connected to a common synchronous clock. The name internal feedback came into existence based upon its XOR connection.

1.1.2 Principle of Operation

The basic block diagram of the LFSR used in this research work is shown in the figure 1.3. The register includes 4 D flip flop with XOR and OR gates. The use of XOR gate can be replaced by even XNOR gate also. Several researches were made in the design of D flip-flop of LFSR register [14, 15] using different logics like pass transistors, NAND, NOR, transmission gates with inverters, domino logic, etc. Though the use of the above logics reduces number of transistors required for D flip-flop and chip size, by eliminating the use of switches to connect supply voltages, there are certain disadvantages in handling the difference of the voltage between high and low logic levels at each stage, as a result the transistors in series is less saturated at its output than at its input.

The tap sequence is the list of bits position that affects the next state. In the block diagram shown, the sequence is [3,4]. The outputs that influence the input are called taps. A maximal LFSR produces
n-sequence (i.e. cycles through all possible 2^n-1 states within the shift register except the state where all bits are zero), unless it contains all zeros, in which case it will never change. Thus the sequence of numbers generated by a LFSR can be considered a binary numeral system just as valid as Gray code or the natural binary code.

![Block diagram of LFSR](image)

**Figure.1.3 Block diagram of LFSR**

The tap sequence of an LFSR must be 1’s or 0’s and so it can be represented as a polynomial mod 2. This is called the feedback polynomial or characteristic polynomial. For the above case, the taps are at the 3rd, 4th, bits the resulting LFSR polynomial is \(X^4+X^3+1\). The powers of the terms represent the tapped bits, counting from the left. If and only this polynomial is a primitive, then the LFSR is maximal. The
LFSR will only be maximal if the number of taps is even. The output sequence is shown in the Table 1.1.

Table 1.1 Binary Numeral Sequence of LFSR

<table>
<thead>
<tr>
<th>Clock Pulse</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>14</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>15</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Q1 - output of flip flop 1  
Q2 - output of flip flop 2  
Q3 - output of flip flop 3  
Q4 - output of flip flop 4
1.2 CMOS VLSI DESIGN

Nowadays static power consumption is considered as a vital design parameter in digital circuits [7, 47] due to emergent usage of mobile products. The increase in static power dissipation during idle mode is all due to the leakage current in sub-threshold region of transistors. The current due to sub-threshold leakage is rises from threshold voltage scaling and gate leakage current increases due to scaling of oxide thickness. Therefore it is very important to consider static power dissipation in the CMOS design flow [46].

1.2.1 Power Dissipation in CMOS Circuits

Power has become a key vital role in the design constraints in all newer CMOS technologies. Power dissipations [79] have materialized due to transistor scaling, chip transistor counts and clock frequencies, in VLSI technology. Major power dissipation in CMOS circuit emerges comes from two components:

- Dynamic dissipation.
- Static dissipation.

1.2.1.1 Dynamic Dissipation

The dynamic power dissipation in the CMOS circuits occurs in the following modes.
Switching transient current

Charging and discharging of load capacitance.

During the transition from either ‘0’ to ‘1’ or, alternatively, from ‘1’ to ‘0’, both n- and p-transistors are on for a short period of time. This results in a short current pulse from VDD to VSS.

Current is also required to charge and discharge the output capacitive load. The current pulse from VDD to VSS results in a “short-circuit” Dissipation that is dependent on the input rise/fall time, the load capacitance and gate design.

\[ P_d = C_L V_{DD}^2 f_p \] \hspace{1cm} (3)

Where

- \( C_L \) : load capacitance
- \( V_{DD} \) : supply voltage.
- \( f_p \) : operating frequency.
- \( P_d \) : dynamic power dissipation

The short circuit power dissipation in the CMOS circuits

\[ P_{SC} = \beta/12 \ (V_{DD} - 2V_t)^3 t_r f / t_p \] \hspace{1cm} (4)

Where

- \( P_{SC} \) : static power dissipation
1.2.1.2 Static Dissipation

Static power dissipation in all the CMOS circuit is due to

- subthreshold conduction through OFF transistors
- tunnelling current through gate oxide
- leakage through reverse-biased diodes
- contention current in circuits

Consider a complementary CMOS gate, if the input='0', the associated n-device is “OFF” and the p-device is “ON”. The output voltage is VDD or logic ‘1’. When the input =‘1’, the associated n-channel devise is biased “ON” and the p-channel device is “OFF”. The output voltage is 0 volts. Note that one of the transistors is always “OFF” when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no DC current path from $V_{DD}$ to $V_{SS}$, the resultant quiescent current, and hence power $P_S$ is zero.

However, there is some small static dissipation due to reverse bias leakage between diffusion regions and the substrate. In addition,
sub threshold conduction can contribute to the static dissipation. It is needed to look at a simple model that describes the parasitic diodes for a CMOS inverter in order to have an understanding of the leakage involved in the device. The source-drain diffusions and the n-well diffusion form parasitic diodes. This can be represented in the profile of an inverter. Since parasitic diodes are reverse-biased, only their leakage current contributes to static power dissipation. The leakage current is described by the diode equation.

\[ I_0 = I_s (e^{\frac{qV}{kt}} - 1) \quad (5) \]

The static power dissipation is the product of the device leakage current and the supply voltage. A useful estimate is to allow a leakage current of 0.1\( nA \) to 0.5\( nA \) per device at a room temperature.

The total static power dissipation, \( P_s \) is obtained from

\[ P_s = \text{leakage current} \times \text{supply voltage} \]

Where

- \( I_s \) - reverse saturation current
- \( V \) - diode voltage
- \( q \) - electronic charge
- \( k \) - Boltzmann’s constant
- \( t \) - temperature.
1.2.2 Delays in CMOS Circuits

The analytic and empirical model that describes the switching characteristics of a CMOS inverter, are used to understand the parameters that affect CMOS delays. More detailed analysis or simulation is usually required to yield models that accurately predict the performances of today’s processes. The switching speed of a CMOS gate is limited by the time taken to charge and discharge the load capacitance $C_L$. An input transition results in an output transition that either charges $C_L$ toward $V_{DD}$ or discharges $C_L$ and $V_{SS}$.

- **Rise time**, $t_r$ = time for a waveform to rise from 10\% to 90\% of its steady-state value.
- **Fall time**, $t_f$ = time for a waveform to fall from 90\% to 10\% of its steady-state value.
- **Delay time**, $t_d$ = time difference between input transition (50\%) and the 50\% output level. Furthermore a differentiation is made between $t_{df}$, the high-to-low delay (input rising), and $t_{dr}$ the low-to-high delay (input falling).
- **Interconnect Propagation Delay**, where Memory cell architectures have unique conditions for interconnect (array-like placement, interconnect with high resistance poly-silicon wires, and high-volume uniform structure) require individual
compensations to ultimately accumulate their effects into a propagation delay model.

1.2.3 Leakage Current Mechanism in CMOS Circuits

These are the three major types of leakage mechanisms [76, 74]:

- Sub-threshold leakage
- Gate oxide leakage and
- Reverse-biased PN-junction leakage.

In addition to these three major leakage components, there are other ones like gate-induced drain leakage (GIDL) and punch through current, which can be neglected in normal modes of operation. However, the VLSI circuit designers have to do accurate and efficient power estimation during the design phase in order to meet the power specification without a costly redesign process. Precise simulators like HSPICE™ can accurately account for leakage current, but they are only proper for small circuits due to convergence, CPU time and memory issues. The physical models to treat the leakage mechanisms are too complex to be used by circuit designers. Faster techniques to estimate the sub-threshold and gate leakage current have also been proposed in various researches. It is important to estimate both average and maximum power in CMOS circuits at different levels of design abstraction. The average power dissipation is
important to determine the battery life, while the maximum power demanded is related to circuit reliability issues.

The power consumption reduction in digital systems involves optimization at different design levels. This optimization includes the technology used to implement digital circuits, the logic style, the circuit architecture, and the algorithm that are being implemented. Optimizations in technology level are related to materials used in the fabrication process, like high-K gate dielectric and metal gates, it is implemented in a parallel architecture and the minimization of the number of operations to reduce the switching activity, and consequently the dynamic consumption.

Leakage mechanism, estimation and reduction techniques will have to be reviewed in three levels including design, architectural and algorithmic levels, in order to provide useful data to the IC designers about leakage currents, dimension and concentration, like oxide thickness and substrate profile, and device structure, like “halo” doping and silicon-on-insulator structures. The CMOS design level involves optimization in physical and logic design including placement, routing and sizing strategy with logic minimization and technology mapping. Architectural level involves performance evaluation in both parallel and pipelined structures to achieve the same performance with a reduced
supply voltage. Algorithm level explores the concurrency to be leakage current in Sub-Micrometer CMOS Gates implemented in a parallel architecture and the minimization of the number of operations to reduce the switching activity, and consequently the dynamic consumption. There are still other leakage components like gate induced drain leakage (GIDL) and punch-through current, which are neglected in normal operation of digital circuits.

1.2.4 Sub-threshold leakage Current

Sub-threshold current [78, 80] occurs between drain and source when transistor is operating in weak inversion region, i.e., the gate voltage is lower than the \( V_{\text{th}} \). Gate Oxide Tunneling Current. Upon scaling down the supply voltage the dynamic power consumption is kept under control, however to maintain a high drive current capability the threshold voltage (Vth) has to be scaled too which increasing sub-threshold leakage currents. Therefore the aggressive device scaling in nanometer regime increases short channel effects such as DIBL and Vth roll-off. To control the short channel effects, oxide thickness must also become thinner in each technology generation. Aggressive scaling of the oxide thickness, in turn, gives rise to high electric field, resulting in a high direct-tunneling current through transistor gate insulator. At circuit level, several techniques to reduce
leakage consumption have been proposed in the literature. To reduce leakage currents, these techniques explore supply and threshold voltage leakage dependence, as well as the concepts of stacking effect and body biasing.

1.2.5 Gate Oxide Tunneling Current

Upon aggressive device scaling in nanometer technology, short channel effects such as DIBL and $V_{\text{throll-off}}$ are raised. To control the short channel effects, oxide thickness must also become thinner in each technology generation. Aggressive scaling of the oxide thickness, in turn, gives rise to high electric field, resulting in a high direct tunneling current through transistor gate insulator. As gate leakage in transistor occurs both during turn ON and OFF condition of transistor, steps have to be taken to reduce it. Reduction is possible only by simultaneous scaling of length, oxide thickness and junction depth of the channel, and considering transistor stacking effect and body effect.

1.2.6 Dual Threshold CMOS

Dual threshold CMOS [17] is a static technique that exploit the delay slack in non-critical paths to reduce leakage power. It offers both high and low threshold voltage ($V_{\text{th}}$) transistors in a single chip that are used to deal with the leakage problem. Fabrication process can achieve a
different $V_{th}$ device by varying different parameters in channel doping profile, channel length modulation, body bias condition, and using a higher gate oxide thickness. Each parameter has its own trade-off in terms of process cost, effect on different leakage components, and short channel effects. As a known fact that high $V_{th}$ transistors suppresses the sub-threshold current, while low $V_{th}$ transistors are used to achieve high performance, for any logic circuit, the transistors in non-critical paths can be assigned high $V_{th}$ to reduce sub-threshold leakage current, while the performance is not sacrificed by using low $V_{th}$ transistors in the critical paths. Therefore, no additional control circuitry is required and both high performance and low leakage power can be achieved simultaneously. Furthermore, dual $V_{th}$ design increases the number of critical paths in a die, decreasing both mean and standard deviation of the die frequency distribution, resulting in reduced performance.

1.3 Supply Voltage Scaling

Supply voltage scaling is used to reduce dynamic and leakage power, and it is used to reduce switching power. It is an effective method of consumption reduction due to the quadratic dependence of the switching power in relation to supply voltage. The supply voltage scaling also provides leakage power savings. By lowering
supply voltage provides an exponential reduction in sub-threshold current resulting from Drain-Induced Barrier Lowering (DIBL) effect. The DIBL effect tends to become more severe with process scaling to shorter gate lengths, therefore power saving will increase with technology scaling. Though this scaling also reduces gate oxide leakage considerably than sub-threshold leakage, circuit performance and logic states are not reliable. Thus optimal point for power savings using this technique is the lowest voltage which the circuit retains its logic states and does not compromise performance.

1.3.1 Static Supply Scaling

In static supply scaling, multiple supply voltages are used. The Critical and non-critical paths and/or units of the design are clustered and powered by higher and lower voltages, respectively. In an extreme case the combinational logic in a circuit can fall to zero when the circuit is in idle mode because it does not need to hold its logic state, increasing the power saving. Whenever an output from a low supply voltage ($V_{DD}$) unit has to drive an input of a high supply voltage ($V_{DD}$) unit, a level conversion is needed at the interface. Furthermore, the secondary voltages could be generated off-chip [31] or regulated on-die from the core supply
1.3.2 Dynamic Supply Scaling

Dynamic supply scaling overrides the cost of using multiple supply voltages by adapting the single supply voltage to the performance demand. When performance demand is low, supply voltage and clock frequency are lowered, delivering reduced performance with substantial power reduction. As mentioned before, this technique gets rid of the cost of using multiple supply voltages. However, the follow overheads are added when this technique is implemented: Circuit has to operate over a wide voltage range; Operating system to intelligently determine the processor speed and voltage regulator to generate the minimum voltage for specific speed.

1.4 VOLTAGE LEVEL CONVERSION

The different voltage levels do not cause any problem in the case of high voltage gates driving low voltage gates. Design techniques for low power consumption in modern VLSI are becoming increasingly important. Power dissipations due to leakage current upon using submicron technology are increasing at dreadful rate.

Articulation of several surveys on CMOS technology indicates that dynamic power is increasing and dominates the leakage current. As supply voltage has not been scaled aggressively enough to keep
power per unit area constant over technology generations, problems in the growth of die area are exacerbated.

1.4.1 Basic Level Converter

Figure 1.4 shows a basic block diagram of level converter [62, 63] operating at different supply voltages, for example one circuit is operating at low supply voltage VDDL while other is operating at high supply voltage VDDH. If the VDDL circuits output is directly connect to VDDH circuit, there will be a static current flow in VDDH circuit from VDDH to GND. In order to overcome these static current, level converter is placed between the VDDL and VDDH circuit. The level converter converts the voltage levels from lower level voltage VDDL to higher level voltage VDDH.

![Basic block diagram of Level Converter](image)

**Figure 1.4 Basic block diagram of Level Converter**

1.4.2 Types of Level Converter

In real time there are many voltage converters are used, they are:

- Standard Level Converter
- Variable Threshold CMOS (VTCMOS) Level Converter
- Multi-threshold CMOS (MTCMOS) Level Converter
1.4.2.1 Standard Level Converter

The standard level converter [16, 17, 18] consists of feedback circuitry between the output and the input side. This circuitry is used when there is a direct connection between a low-swing gate signal and higher supply voltage, for turning ON a pull-up network. The static DC current existing between the input and the output connection has to be controlled. In order to suppress this DC current, feedback-based level converters are used in the connection, which isolates the pull-up network from the low-swing input signal. These traditional level converters, however, suffer from high short-circuit power and high propagation delay due to the typically slow response of the feedback circuitry. Furthermore, the pull-down network in these circuits is driven by low voltage swing signals while the pull-up network is driven by full-swing signals. At very low input voltages, the widths of the transistors that are directly driven by the low-swing signals need to be significantly increased in order to balance the strength of the pull-up and the pull-down networks. This causes further degradation in the speed and the power efficiency of the conventional level converters.

1.4.2.2 Variable Threshold CMOS (VTCMOS) Level Converter

One of the efficient methods [33, 34, 35] to reduce power consumption is to use low supply voltage and low threshold voltage without trailing
the speed performance. But increase in the lower threshold voltage devices leads to increased sub threshold leakage and hence more standby power consumption. Variable Threshold CMOS (VTCMOS) devices are one solution to this problem. In VTCMOS technique threshold voltage of the low threshold devices are varied by applying variable substrate bias voltage from a control circuitry. VTCMOS technique is very effective technique to reduce the power consumption with some drawbacks with respect to manufacturing of these devices. VTCMOS requires either twin well or triple well technology to achieve different substrate bias voltage levels at different parts of the IC. The area overhead of the substrate bias control circuitry is negligible. However, VTCMOS entails additional complexity and overheads due to its triple-well structure and substrate bias voltage generator. Also, the junction leakage and gate tunnel current becomes even worse by the substrate bias.

1.4.2.3 Multi-threshold CMOS (MTCMOS) Level Converter

Multi-threshold CMOS (MTCMOS) [2, 5] is a well known technique to reduce sub-threshold leakage currents [1] during standby modes by utilizing high-threshold voltage (VTH) power switches. In an integrated circuit(IC), there are so many circuits operating at different supply voltages, for example one circuit operating at low supply voltage VDDL
and some other circuits operating at high supply voltage VDDH. If the VDDL circuits output is directly connect to VDDH circuit. Therefore there is a static current flow in VDDH circuit from VDDH to GND. In order to overcome these static current, level converter is placed between the VDDL and VDDH circuits, for converting the voltage levels from lower level voltage VDDL to higher level voltage VDDH.

1.5 OBJECTIVES OF THE THESIS

The aim of this thesis is to analyze performance, area efficiency and power consumption of LFSR counter designed specially using CMOS technology with multi-threshold voltage level converters.

In order to achieve the aim, the following objectives have been set.

i. To design D flip-flop of LFSR counter using few CMOS technologies.

ii. To analyze the CMOS layout results of the D flip-flop designed using the CMOS technologies.

iii. To design the LFSR counter architecture using the efficient D flip-flop design.

iv. To analyze multi-threshold voltage level converters for low and high threshold voltages of CMOS logics.

v. To identify high speed and low-power multi-threshold voltage level converter.
vi. To investigate the optimization and performance of the architectural design.

1.6 ORGANIZATIONS OF THE THESIS

The main work of this research is to investigate and evaluate the performance of CMOS VLSI. The thesis is structured in seven chapters. Chapter 1 gives an overview of LFSR architecture and multi-threshold voltage level converters. Chapter 2 discusses the Extensive study of associated works. Chapter 3 elucidates the proposed LFSR counter design. Chapter 4 presents proposed multi-threshold voltage level converters. Chapter 5 presents the comparative analysis on Proposed Architectural design with previous works. Chapter 6 presents the Results and Discussions of the proposed work. Chapter 7 concludes this work with direction for Future work.
CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

The promising and need based research work is on performance evaluation of CMOS VLSI design. With advancements in large scale integration, millions of transistors are placed on a single chip for complex circuit implementation. Integration leads to several major problems including heat dissipation and power consumption. At the same time as technology moves into deep submicron feature sizes, power dissipation due to leakage current is increasing at an alarming rate. Projections show that leakage power will become comparable to dynamic power dissipation in the next few years. Owing to leakage current dynamic power is increasing, and further dominates in the CMOS technology. Supply voltage has not been scaled aggressively enough to keep power per unit area constant over technology generations. Research has been conducted to solve these problems. Solutions have been proposed to decrease the power supply voltage, switching frequency and capacitance of transistor. The optimal solution for solving these problems is to analyze the performance of VLSI circuit designed using different CMOS technologies for efficient design and
identifying a suitable multi-threshold voltage level converter for the design.

2.2 LINEAR FEEDBACK SHIFT REGISTER (LFSR)

Linear Feedback Shift Register (LFSR) is widely used in many fields including cryptography [66], digital broadcasting and so many communication applications, owing to its simple design, low area overhead, reliability and scaling flexibility.

This register can be formed by performing selective XOR operations on one or more outputs of the flip flop. As the designer can choose the assignment of XOR operations, it is mostly adopted in secured communication fields. Hacking of data pattern generated by the register finds quite difficult owing the user intervention in the design. A detailed literature review is performed on the register design is made in this thesis work.

M. Mahaboob Basha and Towfique Fairooz et al [37] performed LFSR counter analysis using CMOS sub-micrometer, so as to achieve smaller chip size with high operating speeds and efficient usage of energy. The results state that the LFSR counter has more benefits when compared to GRAY & BINARY counter, so it is a new trend setter in the communication field. However the counter suffers some
compromises in area and speed performances, besides high noise immunity.

Seung-Moon Yoo et al [61] used a re-seeding technique to generate input for a new pattern generator using two-level LFSR scheme. The inputs applied are varied and controlled by the counter output. The deterministic seeds computed by the re-seeding technique are loaded into LFSR and the architectural performances were analyzed. The analysis results showed that the LFSR suffered hardware overhead problems upon implementation onto a chip.

L. Feng, X. Wang, and Y. Fang, et al [15] proposed an improved stream cipher based on the linear feedback shift register by adding disturbance on to the initial states. Though there are many advantages like characters of the cipher text correspond to the same characters in the plaintext, there are hindrances in analyzing the statistics data of the characters.

Francois Arnault and Thierry Berger et al [14] made a case study on LFSR using new matrices representation with polynomial fractional coefficients. This new representation leads to sparse representations and implementations and it focused on Windmill LFSRs case for $E_0$ stream cipher. However to achieve an LFSR with a better cost, the
authors must apply their method step by step until XOR operation using their algorithm. An algorithm that construct an LFSR with a given connection polynomial is not existing hence they adjusted it using pick random transition matrix with good properties. As the complexity of this algorithm is driven by the computation of the cofactors matrix and its determinant which can be achieved by a common algorithm, it becomes a time consuming and costly one. Proposed two algorithms one for hardware purpose and other for software purpose to build efficient LFSRs with a low diffusion delay and good implementation criteria. These algorithms are used to link together matrix representations and polynomial representations for efficient LFSMs, LFSRs and windmill LFSRs constructions. These new representations lead to efficient implementations both in software and in hardware. The main drawback is on generalization could be efficiently applied to Feedback with Carry Shift Registers (FCSRs) or to Algebraic Feedback Shift Registers (AFSRs) in several stream ciphers and it is said that Ring LFSRs have always a better diffusion delay with better hardware performances and good software performances, than the proposed one.

Claudio Mucci et al [9] proposed Linear Feedback Shift Registers (LFSRs) for high throughput requirements using parallel implementations accomplished with system on chips (SoCs) and
application specific coprocessors. Initially this register achieves the required performance, upon operation it showed lack of flexibility due to parallelization and the processor performance is limited by the fixed working frequency. The implementation also requires a single operation resulting in variation of throughputs for different look-head factors and block lengths. The synthesis reports suggested that owing to software programmable solution it has a setback while implementing the architecture on to a single silicon chip.

Mohd. Marufuzzaman and H. N. B. Rosly et al [41] made a comparison on LFSR design using NAND gate, transmission gate and pass transistor. The research shows that pass transistor has comparatively smallest power consumption and made LFSR whose inputs and operations are effectively predefined. Some of the outputs are combined in exclusive-OR configuration to form a feedback mechanism. And further designed a high performance level conversion flip flop to reduce the internal switching activities and glitches. A conditional discharged flip flop is used for the level conversion. This flip flop not only reduces the switching activities and glitches, but also reduces the power consumption by reducing the transition delay. The simulation outputs are taken out at 90nm technology, based upon which it is found that only 19% power reduction is achieved.
Dheeraj Kothapalli et al [11] used exclusive-OR whose outputs of two or more of the flip-flops joined together and feeding those outputs back into the input of one of the flip-flops, to form LFSR. The results showed that the propagation delay is reduced with inflation in speed and performance of system; hence the design is implemented using different technologies of CMOS.

M. Kalaiselvi and K.S. Neelukumari et al [25] analysed the LFSR and stated that during scan shifting, more transitions occur in the flip-flops compared to what occurs during normal functional operation. They proposed an encoding scheme which can be used in conjunction with partial LFSR reseeding scheme to significantly reduce test power and test storage. The encoding scheme is provided at the second stage of compression after LFSR reseeding. However it was not successful, as this method can prevent all transitions in the non-transitional blocks and can reduce the number of specified bits for the non-transitional blocks.

H. Lv, Jian-Xia Xie and Jun-Chu Fang et al [23] utilized feedback function of m sequence shift register to create pseudorandom sequences is one critical method to construct desired sequences. Through the feedback functions, the nonlinear maximal length pseudorandom sequences are realized on FPGA. Meanwhile, the
corresponding analysis demonstrates that this type of sequence has ideal pseudorandom characteristic and desirable linear complexity.

N. Mukherjee and J. Tyszer et al [42] stated that ring generators are high-performance linear feedback shift registers capable of handling pseudorandom and deterministic binary sequences. The results show that it has unprecedented speed of operations and a layout-friendly structure. The LFSR is build using a single level of XOR logic, thereby reducing internal fan-out with simple circuit layout when compared to many former designs on linear finite state machines implemented with same characteristic polynomial.

D. Muthiah and A. Arockia Bazil Raj et al [44] provided LFSR architecture with both feed forward and feedback paths, for improving the throughput rate. The architecture was tested using combined parallel and pipelining techniques in order to eliminate the fan-out effect in long generator polynomials. Though this architecture can be applied to any generator polynomial there is a hindrance in area-time product compared to the other designs.

Nahmsuk Oh and Rohit kapur et.al [45] suggested scan chain architecture and algorithm to compute seeds for LFSR, with less computational error. This architecture does not require complex design-for-testability (DFT) for solving linear equations, upon
determination of seeds for test vectors. The compression ratio is slightly lower than the other approaches even though it can handle larger designs in a reasonable amount of time.

Nilesh P. Bobade and Payal A. Malame et al [47] compared several architectures in terms of the hardware implementation, power consumption and CMOS layout, for low power architecture implementation of LFSR Counter in CMOS VLSI. The results concluded that pass transistors are the best for LFSR counter implementation. Thus it is preferable over Gray counters in maintaining the logic density in fabrication process, power optimization, reducing the propagation delay & glitches.

The effective way to reduce power consumption is to use multi-threshold level converters; however the use of this converter may impart delay and energy lose which ultimately decline the potential gain of the integrated system. Sarvesh H.Kulkarni et al [54] implemented level converting circuits that provide either lower energy consumption or better speed. As slower level converters devours timing slack which is need for energy reduction in subsequent gates. The proposed converter reduced the overall power consumption of the circuit and enhances speed upto 25%.
Thomas Johansson and Fredrik Jonsson J. Stern et al [66] proposed novel methods for fast correlation attacks based on identifying an embedded convolution code in the code C generated by the LFSR sequences. While Abdul Razzaq et al [2] offered a novel idea combining the classical encryption technique and LFSR based stream cipher technique for improved security of cipher text. Proposed system generates key stream with very large period size having possibility of key size larger than plaintext. This larger period size provides more encryption security than conventional Vigenere cipher and LFSR based stream ciphers. The proposed solution has been found secure for frequency analysis attack since the key period is larger than plain text. Technique has been analyzed with intentions of cryptanalysis and has been found more secure than traditional techniques. However there is a setback for existing hardware based secure communication.

Balwinder Singh and Sukhleen Bindra Narang et al [6] analyzed the synthesis outputs of low power LFSR architecture in terms of the hardware implementation and power consumption. Based on the comparison result race around condition for the architectures is proposed and it implemented by using 0.13 μm BiCMOS technology provided by IBM. In specific applications, such as $E_0$ stream cipher, the efficiency can be as high as 83% only for certain polynomials. The overlapping between the signals that control the switches for the XOR
operation and the signals used for triggering flip-flops ensures the proper operation of the LFSR, is proposed.

Praveen Kasunde et al [49] proposed a novel test pattern generator suitable for built in self test (BIST) structures used for testing of VLSI circuits. This pattern provides fault coverage with reduced power dissipation. The pattern also reduces the switching activity among the test patterns at the most. The method uses low power linear feedback shift register (LPLFSR) to generate the single input change patterns by XOR operation. The proposed scheme is evaluated by using a 4x4 Braun array multiplier. The System-On-Chip (SoC) approach is adopted for implementation on Altera Field Programmable Gate Arrays (FPGAs) based SOC kits with Nios II soft-core processor. The implementation results, it is verified that the testing power for the proposed method is reduced by very low percentage.

Yanamala Balakrishna et al [73] optimized a Built-In Self-Test (BIST) design based on Linear Feedback Shift Registers (LFSRs) to design several Multipliers and Array Multipliers Architectures. The method provides shorter test time compared to an externally applied test and allows the use of low-cost test equipment during all stages of production. Due to the randomness properties of LFSR this requires very little hardware overhead. The method has focused upon reducing
the switching activity from the test patterns generated from the generator. The huddles in the proposed architecture is power consumption in the generator.

G. Ramesh et al [50] made an analysis on power and area for flip flops used in counters with conventional non-clock gated, conventional clock gated and proposed clock gated techniques. From the experimental result using 0.18µm CMOS technology it is clears that maximum power and area reduction is possible through CMOS counters. Even though power and area reduction is satisfactory, there are hindrances in elimination of redundant transitions and switching power consumption.

M. Janaki Rani et al [20] proposed two techniques such as transistor stacking and self-adjustable voltage level circuit. These techniques are used for reducing leakage power in sequential circuits. The power and delay of three different types of D flip-flops using pass transistors, transmission gates and gate diffusion input gates, analyzed and corresponding circuits were simulated with and without the application of leakage reduction techniques. The simulation results showed that the D flip flop designed using the pass transistor and self-adjustable voltage level circuit has the least leakage power dissipation of 9.13nW with a delay of 77ns, than the other circuits. The
circuits are simulated with MOSFET models of level 54 using HSPICE in 90nm process technology. The leakage power is comparatively high when it is modeled in 90nm technology.

SalendraGovindarajulu et al [53] proposed a new low voltage swing circuit technique based on a dual threshold voltage CMOS technology. The proposed technique is used for simultaneously reducing active & standby mode power consumption and enhancing evaluation speed and noise immunity in domino logic circuits in 65 nm deep submicron technology (DSM). The proposed technique modifies both the upper and lower boundaries of the voltage swing at the dynamic node. Ground, power supply and threshold voltages are simultaneously optimized to minimize the power delay product (PDP). In the deep submicron technology, power delay product must be reduced to increase the efficiency of a circuit. The circuit techniques employing dual thresholds, dual voltages, dual grounds are presented in this work for simultaneously reducing power dissipation and delay in domino circuits and also to increase the noise immunity, however this has hindrances in reduction of power utilization.

2.3 MULTI-THRESHOLD VOLTAGE LEVEL CONVERTER

Application of multiple supply voltages (multi-$V_{DD}$) to any devices or integrated circuits [19, 21] greatly reduces the power consumption of
the integrated circuit without decreasing the circuit speed. Always there is tradeoff between the power consumption and propagation delay, in all CMOS circuits as it uses positive and negative threshold voltages for NMOS and PMOS devices. By use of a common level converter circuit for supplying the threshold voltages, may overcome the hindrances of power and speed factors. In the normal CMOS technology some of the level converters, consumes high power and offers only low speed. The use of multi-threshold based level converter offers high power reduction approximately by 70% and enhancement the speed by 78%, while eliminating the leakage current. Though leakage current in the subthreshold region is eliminated considerably, the circuit produces some short circuit current due to charging and discharging. Research has to be performed to reduce this short circuit current considerable.

Abhishek Kumar et al [1] analyzed the use of Metal gate and High-K dielectric for future transistor, and found that leakage current is the main cause of transistor with SiO2 dielectric. SiO2 dielectric is replaced with High-K dielectric with metal, and further continued scaling. The results showed that k dielectric and found that 300 times improvement in leakage current as well as 100 times improvement in ON/OFF ratio. The most promising candidate (Al2O3) has been found
Al2O3 also show the steeper Sub-threshold swing curve (Faster ON-OFF switching) compare to SiO2.

S. Balakrishna et al [5] provided a fair comparison between standard level converter with feedback network and without feedback network. The presented comparison takes into consideration the behavior and power performance when different data loads are used. The presented simulation results showed that the level converter without feedback network has better performance than the other. A DC current path in CMOS gates driven by low-swing input signals, introduced by the level converter with feedback is suppressed by the level converter without feedback path. The proposed level converter uses transmission gates rather than pass transistor logic.

Artem Sokolov. et al [4] suggested local search and genetic algorithms to test set reordering and perform a quantitative comparison to previously used deterministic techniques. As testing of VLSI circuits can cause excessive heat generation which can damage the chips under test, this algorithm consumes significant dynamic power during testing because of enhanced switching activity in the internal nodes. Further original test is reduced as a dual-objective optimization problem, where switching activity and fault coverage. Hence dynamic power dissipation is reduced considerably, however Pareto-fronts to
the problem of test set reduction is not so successful. Hence test scanning is considered.

W. Aloisi and R. Mita et al [3] proposed gated clock design approach for significant power reduction using specified analytical condition. Simulation results have shown a power reduction of about 10% with a mean error of about 3% with respect to theoretical derivations; however there are drawbacks in validating through many transistor-level.

Yogesh Kumar et al [75] proposed a technique which divides the IC area into regions and then imparts multiple supply voltage (multi-$V_{dd}$) circuit which operates at different voltages. The voltage island is used for supplying necessary supply voltages to all the parts of the IC. By using this voltage island, flow of static current is prevented. The design offers up to 38.10% power reduction and up to 50.88% less Power Delay Product (PDP) than the existing level converters.

Shanky Goyal et al [57] proposed low leakage multi-$V_{th}$ level shifter designed for robust voltage shifting from sub threshold to above threshold domain using MTCMOS technique and sleepy keeper. This approach preferably reduces the leakage current while saving exact logic state. The low-power level shifter using sleepy keeper is
compared with the previous work for different values of the lower supply voltage and performance is analyzed using 45nm CMOS technology, and the results showed that power savings is 37% as compared to the previous work. The circuit when used for sub-threshold to above threshold voltage conversion, it revealed the lowest static power and energy consumption with respect to previous proposed LSs with similar design parameters. However this design has hindrances in speed performance when optimized for low power consumption.

Karthik Naishathrala Jayaraman et al [26] proposed a design of a dual $V_{\text{th}}$ feedback type four-transistor level converter (DVF4) with reduced delay and power overheads. The proposed level converter is based on dual-$V_{\text{th}}$ and feedback technique and is compared to the best available level converter like benchmark circuits. The converter (DVF4) offered significant power savings of 61% over benchmark circuits. A single-$V_{\text{th}}$ alternative of the design is also effective and offers power savings of 56.1% and delay savings of 33.17% for a reduced voltage range. The advantage of DVF4 in dual voltage low power design is demonstrated using various test structures and circuit examples. Optimization of the level converter is made in 32nm CMOS technology, for minimum power consumption and delay. The simulation results showed that this level converter (DVF4) offers power savings up to
53% and delay savings up to 50% over benchmark circuits. Even though the converter has many advantages there is an overhead at the junction of low voltage and high voltage gates.

Suman Nehra et al [64] presented pre-layout simulations of a 3T XNOR cell at low voltages, so as to achieve low power consumption and full voltage swing at low supply voltage. MTCMOS is designed with XNOR rather than XOR gates. Simulation is done by parameter variation for voltage frequency and time. Based upon the simulation results it is concluded that the XNOR gates offers lower power consumption, however it suffered problems in power-delay product and temperature sustainability.

2.4 PERFORMANCE ANALYSIS METHOD

N.A.Doshi et al [12] made a comparative study on LFSR counter designed using components like NAND gates, NOR gates, transmission gates and pass transistors. From the study it was found that the LFSR counter implemented using pass transistor logic yields better results. Though this logic reduces number of transistors required for D flip-flop upon elimination of switches for connecting the supply voltages, there is a major disadvantage in handling the difference of the voltage between high and low logic levels at each stage.
Vikas Sahu and Pradeep Kumar et al [69] compared performance of static LFSR and dynamic LFSR. The comparison results showed that the dynamic LFSRs are preferred in major high performance designs because of its enhanced speed than static LFSR circuits. The performance parameter such as power consumption, delay, and area reduction, leakage current at 90nm, 65nm, 45nm 32nm, and 25nm technologies for high performance LFSR design were analyzed. The performance analysis report showed that pass transistor logic has minimum power dissipation and leakage current, than other logics. However there are many drawbacks while cascading the devices, hence concluded that domino/dynamic logic can be used for designing high performance LFSR.

Ehsan Pakbaznia et al [13] proposed a tri-modal multi-threshold CMOS (MTCMOS) switch design and made a comparison with the similar conventional MTCMOS switches. As this tri-modal switch provides three different power modes for the underlying circuit: active, drowsy, and sleep, data retention ability in the drowsy mode is very excellent, therefore it can be used by candidate for implementing data-retentive power gating designs. Three different low-power design schemes, namely data-retentive power gating, multi-drowsy mode structures, and on-chip dynamic voltage scaling, are implemented
using the proposed tri-modal switch. Based on the analysis report it was found that this tri-modal switch has superior qualities.

The novel test pattern generator for BIST structures for testing of VLSI circuits, proposed by Praveen et al [49] is used in reduction of power dissipation without affecting the fault coverage. The fault existence in the generated test patterns can be reduced by the switching activity of test pattern generator. The single input change patterns generated by a counter and a gray code generator are Exclusive–ORed with the seed generated by the low power linear feedback shift register [LPLFSR]. The projected design is assessed by using a 4x4 Braun array multiplier. The System-On-Chip approach is adopted for implementation on Altera Field Programmable Gate Arrays (FPGAs) based SoC kits with Nios II soft-core processor, reduced to significant percentage.

Marudhai, V et al [39] designed ASIC (Application Specific Integrated Circuit) for LFSRs (Linear feedback shift register) used in cryptography systems (Stream ciphering). As FPGAs have general structure and implementing LFSRs in FPGAs are unable to achieve the required speed, this worked excellent with ASIC based programmable LFSRs and achieved required speed for ciphering data in cryptography. The design is implemented using Cadence tool. The
results showed that maximum frequency and critical path delay are very superior. The design is also verified in both functional and timing simulation.

C. Chen and A. Srivastava et al [8] proposed a technique to optimize power in CMOS digital circuits under the timing constraints, by applying two supply voltages. A technology mapped network is used to analyze the power/delay model and the timing slack distribution in the network. A new strategy was developed for timing-constrained optimization issues, for the power reduction to translate into the polynomial-time-solvable maximal-weighted-independent-set problem on transitive graphs. The use of different supply voltages made to propose a fast heuristic approach to predict the optimum dual-supply voltages by looking at the lower bound of power consumption in the given circuit. Experiment results showed that the resulting lower bound of power is tight for most circuits and that the predicted "optimum" supply voltages are exactly or very close to the best choice of actual ones. The total power saving is only up to 26% without degrading the circuit performance.

P. Corsonello et al [10] proposed an efficient technique for designing high-performance logic circuits operating in subthreshold region. A simple gate-level body biasing circuit is exploited to change
dynamically the threshold voltage of transistors on the basis of the gate status, hence this auxiliary circuit is used to make the logic gate for fast switching while maintaining energy efficiency.

L.H. Pan et al [48] proposed a novel configuration of level shifters for low power application in 0.25 μm technology, for static power dissipation. The circuits utilize the merit of stacking technique by which there is reduction in leakage power. In this work a new level-up shifter designed at ultra low core voltage and has wide range of I/O voltage. The circuit is designed using 0.25 μm CMOS process. Proposed level shifter uses stacking technique to reduce static power dissipation with a little addition in area. Less static power dissipation allow level shifter suitability for wide I/O interface voltage applications in CMOS Technology with very little power dissipation. The results showed improvement in static power dissipation, and have power consumption of 143.193 pw (average) in comparison of conventional level shifter which has static power dissipation i.e. 135.193 pw (average). The area and power consumption have reduced considerably. The major drawback is in leakage power consumption.

B. Sathiyabama et al [55] deployed multiple supply voltages to reduce power consumption without compromising the speed performance parameter of an integrated circuit. Simulation of level
converters is performed in various voltages ranging from 0.4 to 1.5 Volts. Simulation is performed in two phases of high and low voltage levels. The width of the transistor is changed from 2 to 0.5 micrometers to obtain optimized adder using sizing algorithm. The proposed converter has better power efficiency approximately 50% when compared to other existing converters.

K Murali Chandra Babu et al [43] proposed two multi threshold (multi-\(V_{th}\)) level converters without feedback path and compared with conventional level converters. Based on the comparative analysis, he concluded that the proposed level converters offer maximum power saving upto 70% as compared to the previous level converters. The speed factor is said to be enhanced by 78% with proposed one in 90nm TSMC CMOS technology. However there is a setback in area reduction when it is implemented on to the silicon chip.

2.5 NEED FOR THE STUDY

As LFSR is used in a variety of applications such as Built-in-self test (BIST), cryptography, error correction code, pseudo-noise sequence generator and direct-sequence spread spectrum radio, it is much more important to implement LFSR counter architecture in hardware. The existing architecture implemented using counters such as binary and gray suffers with the problem of glitches, power
consumption, speed and delay with increased design complexity and power consumption. The counter is designed using different technologies of CMOS in order to eliminate the propagation delay which decreases the speed and performance of the device.

The utilization of CMOS VLSI in the counter design leads to boost power dissipation due to leakage current and dynamic power at an alarming rate. Owing to the fact that supply voltage has not been scaled aggressively enough to keep power per unit area constant over technology generations, hence there is a trade-off between the power and delay in normal CMOS technology. This snag should be considered in designing the counter using CMOS technology. The using multi-threshold voltage logic can enhance speed and decrease delay. In the normal CMOS technology some of the level converters consume high power and low speed, whereas the multi threshold based level converter offers power reduction by 70% and enhancement in the speed by 78%. A novel low-power architecture using LFSR counter with multi-threshold level converter which reduces the drawbacks of the existing architecture is proposed in this thesis.

2.6 SUMMARY

The literature review is based on CMOS VLSI of LFSR counter architecture and multi-threshold voltage level converter. A meticulous
study on LFSR architectural design using various CMOS logic is made. Study on multi-threshold level converters for low power operation, performance of the architecture and throughput are carried out effectively. The literature survey report elucidates several solutions to be carried out in this research work.
CHAPTER 3

METHODOLOGY

A CMOS design of Linear Feedback Shift Register (LFSR) is taken for the performance evaluation [22, 27], owing to its prevalent usage in a variety of applications. Though a number of architectures for the VLSI implementation of LFSR are reported, it is observed that some of these architectures are of low performance, low throughput, less area efficient and higher cost upon implementation [36]. Therefore a reliable architecture for LFSR with high performance, low-power and cost effective design is needed.

3.1 PROBLEM IDENTIFICATION

Based upon the survey, the following open ended problems have been addressed in this work:

i. The D flip-flop of LFSR is designed using CMOS VLSI logics like NAND gates, NOR gates, Transmission gates with inverters, Static Modified Latches, Pass transistors and dynamic CMOS logic, and layouts were analysed so as to identify area efficient design.

ii. The efficient CMOS logic for the D flip-flop is identified, based on the layout analysis results. The entire LFSR architecture is
designed using the efficient D flip-flop CMOS logic.

iii. High-speed and low-power multi-threshold voltage level converter for the CMOS logic is proposed in order to reduce charge leakage existing in the CMOS circuit due to the unwanted conduction paths.

3.2 SOFTWARE TOOLS USED

i. Digital Schematic Editor
ii. Microwind
iii. HSPICE simulation
iv. XILINX ISE 9.2i
v. Cadence Virtuoso 5.2

3.3 HARDWARE USED

i. Xilinx Spartan 6E Starter Board
ii. FPGA Spartan 3E

3.4 DESIGN OF D FLIP-FLOP USING CMOS VLSI LOGICS

The logic hardware of a LFSR includes components like D flip-flop, OR gates, XOR gates and inverters, out of which D flip-flop considered as the most important component. Among several flip-flops, D flip-flop is considered for LFSR due to its constancy for D inputs in setup and hold-up times. Negative edge triggered
D flip-flop is selected as it inverts the clock input so as to place the signal on falling edge of clock. D flip-flop is designed using several CMOS VLSI logics and power consumption is compared. The D flip-flop is designed using the following devices.

i) NAND gates

ii) NOR gates

iii) Transmission gates with inverters

iv) Dynamic Logic

v) Static Modified Latches

vi) Pass transistors

3.4.1 Design of D flip-flop using NAND Gates

D flip-flop is one of the most common kinds of flip-flops and it is just called as flops or delayed flop. Unlike all other flops it has the ability to retain one bit of digital information and clocking makes it as special D-flop. Figure 3.1 shows the logical design of Master Slave D flip-flop using NAND gates. Operation of the flip-flop depends on the clock pulse. During leading edge of the clock pulse the master flip-flop is enabled and is loaded with data through the D input. Slave is enabled and loaded with the data in the trailing edge of the clock
pulse. Condition when both the flip-flop turn ON is restricted as any one flip-flop will be “ON” while other is “OFF”. Therefore, the output Q acquires the value of D, only when one complete pulse, i.e. 0-1-0 is applied to the clock input. Therefore it is clear that the entire D-FF design needs only eight NAND gates.

Figure 3.1 D flip-flop using NAND Gates

Figure 3.2 Timing Diagram of D flip-flop using NAND gates
Figures 3.2 and 3.3 show the timing and layout diagram of D flip-flop designed using NAND gates. Based upon the layout analysis [16] report it is found that the 17 NMOS transistors and 17 PMOS transistors are needed for the design. The width (W) and length (L) of each NMOS transistor is set at 0.240µm and 0.120µm respectively and its W/L ratio is set at 4/2. The width (W) and length (L) of each PMOS transistor is set at 0.720µm and 0.120µm respectively and its W/L ratio is set at 12/2.

3.4.2. Design of D Flip-Flop using NOR gates

The D flip-flop is designed using three interconnected RS latch circuits all designed using NOR gates. The latch is designed in such a way that the D and D’ signals are separately with the output latch. The D input modifies only the state of lower gates at input circuit, while the
other gates are locked to their output states through interconnections, when the clock pulse is set at logic 0.

When the clock pulse is at logic 1, the circuit immediately forces the output of the two middle input gates to logic 0, hence it is found that the output latch is isolated from any input changes. Based on the state of the D input, any one of the input latches is moved to illegal state and it overrides the latching action of that input circuit. When the clock pulse is set at logic 0, the input latch performing illegal operation will abruptly resume its latching action, and immediately controls the state of the output latch. Owing to this operation the circuit uses an edge-triggered flip-flop for controlling the state of the D input at the moment of the falling clock edge.

Figure 3.4 D flip-flop using NOR gates
The figure 3.4 illustrates NOR-based D flip-flop. When D = 0 and CLK = 1 produces the output Q = 0 and Q! = 1. Also the D = 1 and the CLK = 1 produces the output Q = 1 and Q! = 0. Q! is the complement of Q.

Figure 3.5 Timing diagram of D flip-flop using NOR gates

Figure 3.6 Layout of D flip-flop using NOR gates
Figures 3.5 and 3.6 illustrate the timing diagram and layout diagram of D flip-flop designed using NOR logic gates. Upon analyzing the layout it is found that 13 NMOS transistors and 13 PMOS transistors are needed for designing the D flip-flop using NOR gates. The width (W) and length (L) of each NMOS transistor is set at 0.240µm and 0.120µm respectively and its W/L ratio is set at 4/2. The width (W) and length (L) of each PMOS transistor is set at 0.720µm and 0.120µm respectively and its W/L ratio is set at 12/2.

3.4.3 Design of D FLIP-FLOP using Transmission gates with Inverters

![Diagram of D flip-flop using Transmission gates with Inverters]

**Figure 3.7 D flip-flop using Transmission gates with Inverters**

The figure 3.7 shows the D flip-flop designed by using Transmission
gates and Inverters. The design includes four transmission gates (T1 to T4), four inverters (I1 to I4) and two NMOS transistors. At negative clock edge, transistors [67, 68] T1 and T4 are switched ON and transistors T2 and T3 are switched OFF, hence the previous triggered values from the D_in are stored in the slave through two inverters I3, I4 and T4.

However the master could not latch the next state as T3 is OFF. During the positive clock edge transistors T2 and T3 are turned ON and new latched value is passed to slave through I1, I2 and T2. To reset the flip-flop circuit, both the master and slave circuits are ground.

Figure 3.8 Timing diagram of D flip-flop using Transmission gates with Inverters
Figures 3.8 and 3.9 illustrate the timing diagram and layout diagram of D flip-flop designed using transmission gates with inverters. The analysis report indicates that 14 NMOS transistors and 12 PMOS transistors are needed in the design. W/L ratio of two NMOS transistors is set as 17/2 while all other NMOS are set at 4/2, in order to retain the charge for a long period. However there is no change in the width and length ratio for PMOS and it is set at 12/2.

3.4.4 D flip-flop designed using Dynamic Logic

The figure 3.10 represents the D flip-flop that is designed using dynamic logic. The dynamic logic requires a minimum clock rate which
is fast enough for each dynamic gate to transit its output before it leaks out of the capacitance holding that state. As the output of logic is not driven actively during the part of the clock cycle, the errors due to improper transition is avoided, therefore when the dynamic logic if properly designed, can be operated twice as fast as static logic.

When clock phase $\Phi$ is set at logic 1, the master is set active and the output voltage is set by D. If $D = 1$ and $V = V_{DD}$ the present state output is logic 0 which when fed to next slave stage produces logic one at Q, similarly when the D input is logic 0 it produces logic 0 at the Q output.

![D flip-flop Using Dynamic Logic](image)

Figure 3.10 D flip-flop Using Dynamic Logic
The figure 3.11 indicates the timing diagram of Dynamic Logic based D Flip flop. The diagram clearly depicts that when D input is logic ‘1’ then Q output is also logic ‘1’.
The schematic diagram of D flip-flop using dynamic logic shown in the figure 3.12 indicates that 5 NMOS and 5 PMOS transistors are used in the design. The MOS devices are selected according to the requirements, so each has different width-length ratios. Figure 3.13 depicts the Layout diagram of Dynamic Latch based D flip-flop, with different width-length ratio.

Figure 3.13 Layout diagram of Dynamic Latch based D flip-flop

3.4.5 Design of D flip-flop using Modified static latch

This latch circuits has its output connected to the ground. Latches are used for storing data temporarily. It draws additional current for its large internal capacitances, hence the overall power consumption is more with high delay time and high noise margin. The design uses latches to introduce valuable delays. When the D = 0 and the
CLK = 1 produces the output Q = 0 and Q’ = 1. Also the D = 1 and the CLK = 1 produces the output Q = 1 and Q’ = 0. Q’ is the complement of Q.

**Figure 3.14 D flip-flop using Modified static latch**

Figures 3.15 and 3.16 show the timing and layout diagrams. Based upon the report it is determined that modified static latches uses 6 NMOS transistors and 6 PMOS transistors for designing D flip-flop, and all the MOS device do not have same W/L ratio. Hence the area occupied by the design is more compared to dynamic logic.
Figure 3.15 Timing diagram of D flip-flop using Static Modified Latches

Figure 3.16 Layout of D flip-flop using Static Modified Latches
3.4.6 Designing D flip-flop using Pass transistors

The use of pass transistor in D flip-flop design is assumed to be one among several simplest designs. The figure 3.17 depicts the design of D flip-flop using pass transistors. When clock pulse is at logic 0, the PMOS loop transistor is ON and the two chained inverters are in memory state, while others at OFF state. Upon grounding the master and slave devices, reset operation is made.

Figure 3.18 Timing diagram of D flip-flop using Pass transistors
Figure 3.18 shows the timing analysis of D flip-flop designed using pass transistors. The figure 3.19 shows the layout diagram of the D flip-flop. This layout report pin points the channel length and width dimensions of each of the n type and p type MOS transistor. The D flip-flop using pass transistor is designed using 9 NMOS transistors and 5 PMOS transistors. The NMOS transistors does not have identical width-length ratio, however it differs to 30%. The advantages of pass transistors are that there is no direct path between voltage supply and ground, hence do not dissipate standby power. The pass transistors are used as function block and it is potentially very efficient with layout results. As pass transistors can usually be minimum size, the chip is very less. Propagation delays can become large in long series strings of pass transistors. Static power dissipation is unaffected. Dynamic power dissipation may be decreased. The major disadvantage of pass transistor logic circuit is that if the threshold voltages of all transistors are same, then the node voltage at the end of the pass transistor chain will become one threshold voltage lower than $V_{DD}$, regardless of number of pass transistors in chain. A CMOS is a combination of both N and PMOS transistors, if the threshold voltage supplied to the integrated circuit performs malfunctioning, then entire logic operations goes wrong. To overcome this problem multi-threshold logic is suggested.
3.5 COMPARATIVE ANALYSIS OF D FLIP-FLOP DESIGN

The D flip-flop known as the seed for LFSR counter is designed using NAND gates, NOR gates, Transmission gates with inverters, Dynamic logic, Static modified latches and Pass transistors. The table 5.3 illustrates the comparative study of D flip-flop design using various logics. Based upon the statistical data is it clear that dynamic logic and pass transistor logic are preferred over other logics due to it minimum usage of transistors. Table 3.1 shows the comparative analysis specifying usage of MOS transistors for the D flip-flop design.
Table 3.1 Analysis of D flip-flop designed using various logics

<table>
<thead>
<tr>
<th>S.NO</th>
<th>USED LOGIC</th>
<th>NO.OF NMOS DEVICES</th>
<th>NO.OF PMOS DEVICES</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>NAND gates</td>
<td>17</td>
<td>17</td>
</tr>
<tr>
<td>2.</td>
<td>NOR gates</td>
<td>13</td>
<td>13</td>
</tr>
<tr>
<td>3.</td>
<td>Transmission gates with inverters</td>
<td>14</td>
<td>12</td>
</tr>
<tr>
<td>4.</td>
<td>Dynamic Logic</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>5.</td>
<td>Static Modified Latches</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>6.</td>
<td>Pass transistors</td>
<td>9</td>
<td>5</td>
</tr>
</tbody>
</table>

The figure 3.20 shows the analysis of NMOS device used in the
D flip-flop design. NMOS device has a positive threshold voltage and uses chip area minimum compared to the PMOS devices. The total number of NMOS in D flip-flop designed using pass transistor logic and dynamic logic design are very less when compared with other logics. However owing to the known drawbacks of pass transistor logic, dynamic logic is well preferred to design the D flip-flop. The use of this dynamic logic greatly reduces the static DC paths between the supply and ground lines.

Figure 3.20 Analysis of NMOS device in D flip-flop design
Figure 3.21 Analysis of PMOS device in D Flip flop design

The figure 3.21 shows the analysis of PMOS device used in the D flip-flop design. As CMOS logic uses both NMOS and PMOS devices, the design parameter of PMOS devices is also very important as that the NMOS devices. The total number of PMOS devices used in NAND gate logic is 17, NOR gate logic is 13, and transmission gates with inverter logic are 12. The analysis reports showed that pass transistor logic and dynamic logic used only 5 and whereas the modified logic used 6 devices. The use of this dynamic logic greatly preferred over the pass transistor logics. The analysis report showed that the dynamic logic is well preferred to design the LFSR counter architecture, in view of the fact that the number MOS transistors to be used are very less. As only 5 NMOS devices and 5 PMOS devices are
utilized, the total power consumed by the logic is extremely minimum and the chip area occupied by the device is also very minimum.

### 3.6 LFSR COUNTER ARCHITECTURE USING DYNAMIC LOGIC

Dynamic LFSRs are most widely used in recent VLSI circuits, even though domino LFSR has wide fan-in logic in high-performance applications. These dynamic LFSRs are often favored in high performance designs because of the speed advantage offered over static LFSR circuits. The performance parameters such as power consumption, propagation delay and leakage current of the design is compared with other LFSR at 65nm, 45 nm, 32 nm and 25nm technologies to identify high performance LFSR design.

![Figure 3.22 Dynamic Logic based LFSR counter architecture design](image)
The figure 3.22 shows the schematic diagram of a dynamic logic based LFSR counter design. The outputs out3 and out4 are combined using exclusive-OR configuration to form a feedback mechanism and can be fed back as the input to the first flip-flop as shown in the figure. Dynamic logic circuits offer several advantages in realizing high density, high performance digital system where reduction of circuit delay and silicon area is important.

Operation of all dynamic logic gates does not depend on steady-state circuit behavior, however it rely on temporary storage of charge in parasitic node capacitances. It uses periodic clock signals for controlled charge refreshing. Use of common clock signals the system enables synchronize the operation of various circuit blocks. Capability of temporarily storing a state at a capacitive node allows implementing simple sequential circuits with memory functions. Hence this logic reduces usage of chip area by using less number of transistors per gate, while reducing power utilization.

From the figure 3.23 and from the layout analysis data sheet, it is clearly depicted that the LFSR counter using dynamic logic is designed using 20 NMOS transistors and 20 PMOS transistors with specified dimensions. As minimum number of transistors is used when compared to pass transistor based LFSR counter, power consumption
and chip area occupied by the design will also be reduced considerably. However there is a slender charge leakage in the CMOS circuits due to the superfluous conduction paths like subthreshold and reverse junction currents. The use of small-sized, leaky capacitors for storing logic values, and pre-charging the output node according to the inputs, are the setbacks in the LFSR design. These setbacks are overcome by use of an efficient multi-threshold voltage level converter.

Figure 3.23 Layout diagram of LFSR counter using Dynamic Logic

3.7 SUMMARY

After analyzing all the design of D flip-flop, it is very clear that the dynamic logic is preferred to design the D flip-flop. This design uses 20 NMOS and 20 PMOS devices, which are comparatively very less than
the other logics. It utilizes less number of MOS transistors, therefore the chip area occupied by the design is said to be minimum. As the design uses less number of transistors and uses minimum chip area, power consumption is considerably reduced. Owing to many advantages, the dynamic logic is preferred to design the D flip-flop of LFSR counter architecture; however there will be a slender charge leakage exists in the CMOS circuits due to the surplus conduction paths like subthreshold and reverse PN-junction currents which cannot be eliminated. The logic uses a synchronous internal clock whose clock frequency must set at high level to induce a latching current before the charge state changes. A multi-threshold voltage level converter with best efficiency has to be utilized to overcome these setbacks.
CHAPTER 4

MULTI-THRESHOLD VOLTAGE LEVEL CONVERTER

4.1 INTRODUCTION

With advancements in large scale integration, millions of transistors can be placed on a single chip for implementation of complex circuitry. As a result of placing so many transistors in such a small space, major problems of heat dissipation and power consumption have come into the picture. According to Gordon Moore law the number of transistors in a die is increasing exponentially with time, so the power consumption of the die increases, area of the die also increases and automatically the performance of the die is also decreasing. In order to overcome the certain drawbacks scale down the device dimensions.

Research has been conducted to solve these problems. Solutions have been proposed to decrease the power supply voltage, switching frequency and capacitance of transistor. The optimal solution for solving these problems is to analyze the performance of VLSI circuit designed using different CMOS technologies. More and faster transistors are crammed onto integrated circuits with each new technology generation. The increased number of transistors and the enhanced clock frequency lead to a significant increase in the power consumption with each new technology generation. Furthermore,
deviation from the constant field scaling due to the non-scaling parameters of the MOS transistors (the thermal voltage, the silicon energy band gap, and the source/drain doping levels) leads to an increase in the power density. The higher power dissipation coupled with the imbalanced utilization and the diversity of circuitry elevates the temperature and produces local hot-spots across a die. The increased power dissipation degrades the reliability, increases the cost of the packaging and cooling system, and lowers the battery lifetime in portable electronic devices.

An effective method for reducing the power consumption is scaling the supply voltage. Dynamic, short-circuit, and leakage components of power consumption are simultaneously reduced with the scaling of the supply voltage in a CMOS circuit. Lowering the supply voltage, however, also degrades the circuit speed. The multi-circuit technique exploits the delay differences among the different signal propagation paths within an integrated circuit (IC).

The supply voltages of the gates on the noncritical delay paths are selectively lowered while a higher supply voltage is maintained on the critical delay paths in order to satisfy a target clock frequency in a multi-circuit (LFSR counter). Similarly, in systems-on-chips (SoCs), different circuits operating at different supply voltages exist. When a
low voltage swing signal drives a CMOS gate connected to a higher supply voltage, static dc power is consumed as the transistors in the pull-up and the pull-down networks are simultaneously turned on. Furthermore, the output voltage swing of the receiver degrades, thereby leading to a static dc current in the fan-out gates of the receiver. In order to transfer signals among these circuits operating at different voltage levels, specialized voltage interface circuits are required.

4.2 MULTI-THRESHOLD VOLTAGE (MULTI-$V_{\text{th}}$)

In typical all CMOS circuits have pull-up and pull-down networks consisting of PMOS and NMOS transistors, respectively. Owing to use of both P and N devices in the same logic, there becomes a need for dual threshold voltages [18] with proper level converters [29, 31, 32]. The multi-threshold CMOS (MTCMOS) [40, 62, 65] is a very attractive technique to reduce sub-threshold leakage currents during standby modes by utilizing high-$V_{\text{th}}$ power switches. This technology is straightforward to use, because existing designs can be modified to become MTCMOS blocks by simply adding high-$V_{\text{th}}$ power switches. In addition, circuits can easily be placed in low leakage states at a fine grain level of control. Several computer-aided methodologies have been proposed in the literature to optimally design MTCMOS circuits.
Some of those methodologies employed high-$V_{th}$ switch sleep transistors, whereas others have involved embedded high-$V_{th}$ transistors or gates.

A major goal of the technology scaling [28, 30] trend is to reduce the gate delay by 30%, and to double the transistor density by CE scaling. In addition, a 50% reduction in power can be achieved by a basic shrink at the CE scaling. Power reduction [56, 58] is an important design criterion to satisfy, especially for battery operated systems. As a result, more aggressive ($V_{DD}$-$V_{th}$) scaling will be important to minimize power consumption. Lowering the power supply is the most effective way to reduce power dissipation, because the dynamic switching energy is proportional to the square of the supply voltage. To maintain performance during voltage scaling, the threshold voltage is scaled as well, in order to achieve a large enough gate overdrive. It can be seen how an intrinsic gate speed can be maintained by scaling both $V_{DD}$ and $V_{th}$ as shown in the following.

$$T_{pd} \propto C_L V_{DD}/(V_{DD} - V_{th}) \alpha \quad ------ (6)$$

Where

- $T_{pd}$ - gate propagation delay.
- $\alpha$ - models short-channel effects.
- $C_L$ - load capacitance.
\[ V_{th} \] - Threshold voltage
\[ V_{DD} \] - Supply voltage

The increase in sub threshold leakage energy is small compared to the quadratic reduction in sub threshold leakage energy is small compare to the quadratic reduction in the dynamic power supply due to \( V_{DD} \) scaling for modern CMOS technologies. With further \( (V_{DD} - V_{th}) \) scaling, increase in leakage current can start to dominate the reduction.

This indicates that there must be an optimum \( V_{th} \) point, and consequently, a \( V_{DD} \) point for a given delay. For a given process and \( V_{DD}/V_{th} \) ratio, the energy efficient (and corresponding \( V_{DD} \)) point is significantly below the typical threshold levels of today’s technologies. This excessive headroom indicates that there is still room for optimal \( (V_{DD} - V_{th}) \) scaling to lower overall power dissipation. But, lowering threshold voltages has several undesirable consequences. Noise margins, short-channel effects, and \( V_{th} \) variations all become worse with lower threshold voltages, and must be carefully balanced with may be gained in the overall power dissipation.

4.2.1 Embedding Multi-\( V_{th} \) CMOS Design in Level Converters

The static approach does not employ any control signals for power savings. In the static multi-\( V_{th} \) technique, gates off the critical paths are
designed to operate at a high-$V_{th}$ in order to reduce leakage power without the performance being affected. Yet, gates lying on critical path operate at a low-$V_{th}$ to maintain high performance. It should be pointed out that in aggressive high-performance low-power circuit topologies that have several balanced critical paths, many gates cannot be slowed down only a limited leakage reduction can be achieved.

However in Dynamic threshold CMOS, body and gate of an MOS transistor are tied together and the threshold voltage is varied dynamically to suit the circuit’s operating state. The threshold voltage of the device is lowered during switching, thereby increasing the transistor drive current. However, the threshold voltage is increased during the standby mode, limiting the leakage current. The DTCMOS technique is limited to supply voltages of less than 0.6v to prevent the forward bias well-to-source junction.

Level converters impose additional power consumption and propagation delay overhead in a multi- system. High-speed and low power voltage interfacing is critical for effective power reduction with minimum effect on speed in a multi-IC. Several factors such as the path propagation delay statistics, the power and delay overhead of the level converters, and the availability and efficiency of the different power supplies determine the choice of the supply voltages in a
multi-system. The number and the voltages of the multiple power supplies therefore vary with the type of the IC and the target set of applications.

Allowing designers to assign the low-threshold devices to critical paths and utilize high-threshold devices for non-critical paths. Alternatively, some experimental designs are now being reported which utilize dual (or triple) supply voltages. The overall goal with low-power design is to identify any slack timing available, then eliminate this slack timing while saving power through the use of lowered supply voltage, increased threshold voltage, or smaller transistor sizes. Typically, this is achieved through the use of either a dual-\(V_{th}\) process or dual-\(V_{DD}\) design, along with sizing.

### 4.3 STANDARD LEVEL CONVERTERS

Figure 4.1 shows a Dual \(V_{DD}\) CMOS circuit each operating at different supply voltages for example one circuit is operating at low supply voltage \(V_{DDL}\) while other is operating at high supply voltage \(V_{DDH}\). If the \(V_{DDL}\) circuits output is directly connect to \(V_{DDH}\) circuit, there will be a static current flow in \(V_{DDH}\) circuit from \(V_{DDH}\) to GND, due which power consumption increases with increase in power delay product in the circuit. In order to overcome these static current, level converter [63, 65] is placed between the \(V_{DDL}\) and \(V_{DDH}\) circuit. Figure 4.2
shows the basic block diagram of level converter. These level converter converts the voltage levels from lower level voltage $V_{DDL}$ to higher level voltage $V_{DDH}$.

![Diagram of Dual $V_{DD}$ CMOS Circuit](image1)

**Figure 4.1 Dual $V_{DD}$ CMOS circuit**

![Diagram of Basic Block Diagram of Level Converter](image2)

**Figure 4.2 Basic block diagram of Level Converter**
4.3.1 Level Converter with Feedback Loop

The conventional feedback-based level converters [67, 68] are discussed in this section. When a low swing signal directly drives a gate that is connected to a higher supply voltage, the pull-up network of the receiver cannot be fully turned off. A receiver driven by a low voltage swing signal therefore produces static dc current. In order to suppress this dc current, specialized voltage interface circuits are employed between a low voltage driver and a full voltage swing receiver, in the standard feedback-based voltage interface circuits.

The pull-up network transistors are not directly driven by the low voltage swing signal provided driver. The operation of the pull-up network transistors is controlled by an internal feedback mechanism isolated from the low voltage swing input signal, thereby avoiding the formation of static dc current paths within the circuit. These traditional level converters, however, suffer from high short-circuit power and long propagation delay due to voltages from the full-voltage swing feedback paths.

Particularly, at very low input voltages, the widths of the transistors that are directly driven by the low-swing signals need to be significantly increased in order to balance the strength of the pull-up and the pull-down networks.
This causes further degradation in the speed and the power efficiency of the conventional level converters when utilized with very low input voltages. The standard feedback-based level converter (LC1) is shown in figure 4.3. M1 and M2 experience a low gate overdrive voltage \((V_{DDL} - V_{TH})\) during the operation of the circuit. M1 and M2 need to be sized larger to produce more current as compare to M3 and M4, respectively for functionality. The circuit operates as follows. When the input is at 0V M2 is turned off. Node1 is charged to \(V_{DDL}\). Node3 is discharged to 0V turning M4 on. Node2 is charged to \(V_{DDH}\) turning M3 off. The output is pulled down to 0V. When the input transitions to \(V_{DDL}\), M2 is turned on. Node1 is discharged, turning M1 off. Node2 is
discharged, turning M3 on. Node3 is charged up to $V_{DDH}$ turning M4 off. The output transitions to $V_{DDH}$.

A feedback loop, isolated from the input, controls the operation of M3 and M4 during both transitions of the output. Due to the transitory contention between the pull-up and the pull-down networks and the large size of the NMOS transistors (M1 and M2), however, LC1 consumes significant short-circuit and dynamic switching power. To maintain functionality with the lower values of $V_{DDL}$, the sizes of M1 and M2 need to be further increased in order compensate for the gate overdrive degradation. The load seen by the previous stage (driver circuit) is therefore increased, thereby further degrading the speed and increasing the power consumption. Tapered buffers are required to drive M1 and M2 at very low voltages. These tapered buffers further increase the power consumption of LC1. The major disadvantages are Long propagation delay and short circuit current.

4.3.2 High Speed Level Converter

Another level converter (LC2) [63, 72] is presented for enhanced speed as compared to LC1. LC2 is shown in the figure 4.4. M6 maintains the voltage of Node3 between $V_{DDL}$ and $V_{DDL} + V_{TH}$ in order to enhance the current produced by M1. The capacitor C=8pF stabilizes the voltage of Node3 against the noise induced by the
nearby switching events. The circuit operates as follows. When the input is at 0V, Node1 is discharged through M1. M3 is turned on. M2 is turned off. Node2 is charged to $V_{DDH}$, turning M4 off. The output is discharged to 0V. When the input transitions to $V_{DDL}$, M2 is turned on. Node1 is initially charged to a voltage between $V_{DDL} - V_{TH}$ and $V_{DDL}$ through M1.

M3 is not completely cut off (weakly active). M2 is sized to be stronger than M3 for the circuit to function properly. Node2 is discharged, turning M4 on. Node1 is charged all the way up to $V_{DDH}$, thereby eventually turning M3 off. The output transitions to $V_{DDH}$. When the input switches from 0V to $V_{DDL}$ there is a direct current path from $V_{DDH}$ to GND through the M2–M3 path. This direct current path exists until Node1 is charged to $V_{DDH}$ through M4 and M5. Similarly, when the input switches from $V_{DDL}$ to 0V, there is a direct current path from $V_{DDH}$ to GND through the M5–M4–M1 path.

This direct current path exists until Node2 is pulled up to $V_{DDH}$ and M4 is turned off. LC2 therefore consumes significant short-circuit power, similar to LC1, during both low-to-high and high-to-low transitions of the output. This direct current path exists until Node2 is pulled up to $V_{DDH}$ and M4 is turned off. LC2 therefore consumes significant short-circuit power, similar to LC1, during both low-to-high.
and high-to-low transitions of the output. Furthermore, when $V_{DDL}$ is reduced, a significant increase in the size of M2 is required for maintaining functionality. The load seen by the driver circuit therefore increases at Lower $V_{DDL}$. Tapered buffers are driving LC2 at very low voltages. The circuit has several advantages like enhanced speed, leakage current reduction, and there is disadvantage like short circuit current due to charging and discharging.

Figure 4.4 High speed level converter (LC2)

4.4 PROPOSED MULTI-THRESHOLD VOLTAGE LEVEL CONVERTER

4.4.1 Multi-$V_{TH}$ based level converter (PC1)

The proposed level converters employ a multi-$V_{TH}$ CMOS technology in order to eliminate the static dc current, without using feedback path. The high threshold voltage pull-up network transistor in the level
converter is directly driven by the low-swing signals without producing a static dc current problem.

![Multi V\textsubscript{TH} based level converter (PC1)](image)

**Figure 4.5 Multi V\textsubscript{TH} based level converter (PC1)**

PC1 is composed of two cascaded inverters with dual-V\textsubscript{TH} transistors. The threshold voltage of M2 (V\textsubscript{TH-M2}) is more negative (higher V\textsubscript{TH}) for avoiding static dc current in the first inverter when the input is at V\textsubscript{DDL}. V\textsubscript{TH-M2} is required to be higher than V\textsubscript{DDH}-V\textsubscript{DDL} for eliminating the static dc current. PC1 operates as follows:

When the input is at 0 V, M2 is turned on. M1 is cutoff. Node1 is pulled up to V\textsubscript{DDH}. The output is discharged to 0V. When the input transitions to V\textsubscript{DDL}, M1 is turned on. M2 is turned off since V\textsubscript{GS},
M2>V_{TH}, M2. Node1 is discharged to 0V. The output is charged to $V_{DDH}$. PC1 has fewer transistors as compared to LC1 and LC2. Furthermore, the elimination of the slow feedback circuitry reduces the short-circuit power of PC1 as compared to LC1 and LC2. For the lower values of $V_{DDL}$, the threshold voltage of M2 needs to be more negative (higher-$V_{TH}$) in order to suppress the static dc current. Provided that a Multi-$V_{TH}$ CMOS technology is available, no increase in the size of M1 is required for achieving functionality at lower input voltages with the proposed circuit (unlike LC1 and LC2). Therefore, particularly for the very low values of $V_{DDL}$, PC1 consumes lower power, occupies significantly smaller area, and imposes a much smaller load capacitance on the input driver as compared to LC1 and LC2.

**4.4.2 Multi-$V_{TH}$ based High Speed Level Converter (PC2)**

Figure 4.6 describes the Multi-$V_{TH}$ based high speed level converter [58]. The circuit includes four MOS devices out of which M2 requires high threshold voltage than $V_{DDH}-V_{DDL}$ to eliminate the static dc current when the input is low (Node1 is at $V_{DDL}$). M1 needs to be cutoff after a “1” is successfully propagated to the output. The input is at $V_{DDL}$ and the output is at $V_{DDH}$. In order to avoid the formation of a static dc current path between $V_{DDH}$ and $V_{DDL}$ through M1.
The peripheral circuitry composed of M3, M4, and C, is employed to maintain the Node2 voltage. In order to enhance the speed of charge transfer through M1 while avoiding the formation of a static dc current path within the level converter, M3 maintains the voltage of Node2 at cutoff under normal operating conditions with no external noise coupling onto Node2. The purpose of M4 is to provide a discharge path for Node2 if the voltage on Node2 temporarily exceeds $V_{DDL} + V_{TH}$ - M4 due to nearby switching events and crosstalk, while capacitor (C=6pF) stabilizes the voltage of Node2 against the noise induced by the nearby switching events.

![Multi-V_{TH} based high speed level converter](image)

**Figure 4.6 Multi-V_{TH} based high speed level converter**
Figure 4.7 Modified Multi-$V_{TH}$ based high speed level converter (PC2)

Figure 4.7 shows modified Multi-$V_{TH}$ based high speed level converter (PC2). The circuit shown in the figure 4.6 is modified for handling the very low values of $V_{DDL}$. The uncertain values of $V_{DDL}$ and $V_{DDH}$ is handled by direct connection of $V_{DDL}$ to M2, thereby eliminating the static current path.

PC2 is operated as follows: When the input is at 0 V, M2 is made OFF due to $V_{DDL}$, hence the output node is discharged to 0V through the pass transistor M1. When the input transits to $V_{DDL}$, output node is initially charged to $V_{DDH} - V_{th}$, and $V_{DDL} - V_{th}$-M1 through M1, M2 is turned ON after the high-to-low propagation delay of the inverter (I1). The output is pulled high all the way up to $V_{DDH}$ through
M2. M1 is turned off isolating the two power supplies. Both M1 and M2 assist the output low-to-high transition, thereby eliminating the contention current and enhancing the low-to-high propagation speed. The small transistor count and the elimination of feedback loop, reduces the power consumption of this level converter as compared to LC1 and LC2.

4.4.3 Low Power Level Converter (PC3)

The measure of propagation delay includes the loading effect of the level converter on the driver circuit upon optimization. Reduction in size of the transistor decreases the dynamic switching power consumption by lowering the switched capacitance, and increases the output rise and fall times which consequently increases the short-circuit power consumption of the load (IL).

![Figure 4.8 Low Power Level Converter (PC3)](image)

Figure 4.8 Low Power Level Converter (PC3)
A Low power level converter (PC3) shown in the figure 4.8 is proposed in order to overcome the tradeoff between the dynamic switching power consumption of the level converter and the short-circuit power consumption of the load. This circuit consumes less power compared to other level converters (PC1, PC2), and enhances the speed of the level converter. This low-power level converter circuit is optimized with two different design criteria for each value of $V_{DDL}$. When the $V_{DDL}$ is very low, the level converter provides high power with the use of MN1, owing to this output rise time and fall times are increased with reduced number of transistors. The design and optimization of the circuits are carried out at 0.18µm TSMC CMOS technology. This converter minimizes the average power consumption and average propagation delay.

**Table 4.1 Power Analysis of level converter PC3**

<table>
<thead>
<tr>
<th>$V_{DDL}$</th>
<th>$V_{DDH}$</th>
<th>Power in µ watts</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5V</td>
<td>1.8V</td>
<td>0.0057</td>
</tr>
<tr>
<td>1.0V</td>
<td>1.8V</td>
<td>1.0485</td>
</tr>
<tr>
<td>1.2V</td>
<td>1.8V</td>
<td>0.7861</td>
</tr>
</tbody>
</table>
The above table 4.1 illustrates the power analysis of level converter (PC3). The average power consumed by the level converter during 0.5V $V_{DDL}$ and 1.8V $V_{DDH}$ is very less and it in the range specified in microwatts. However the power is higher during 1V $V_{DDL}$ and 1.8V $V_{DDH}$ range.

Figure 4.9 Power Analysis of level converter

Graphical representation of power analysis data for proposed level converter PC3 is shown in the figure 4.9. The graph indicates that the power utilized in conversion of voltage in 0.5V and 1.8V range is comparatively very less in the order of nanowatts. As this level converter uses only minimum number of transistors with no feedback path between the output and input, power utilized by the converter
logic is very less when compared to other conventional level converters with feedback path. Elimination of feedback path reduces the leakage static charges in the logic. Owing to this advantage it is well suited for the proposed LFSR counter architecture.

**Table 4.2 Chip Area analysis of the level converters**

<table>
<thead>
<tr>
<th>S.NO</th>
<th>LEVEL CONVERTER</th>
<th>CHIP AREA ($\mu$m$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PC1</td>
<td>32</td>
</tr>
<tr>
<td>2</td>
<td>PC2</td>
<td>36</td>
</tr>
<tr>
<td>3</td>
<td>PC3</td>
<td>30</td>
</tr>
</tbody>
</table>

The table 4.2 illustrates the comparative analysis of used chip area of all the three voltage level converters. The level converters are designed and simulated. According to the synthesis report, it is found that the proposed level converter PC3 offers lower chip area when compared to the other devices. Though the level converter PC1 has very simple design structure, it use higher chip area. Though the converter PC2 has high efficiency with good performance, the chip
area utilization is more than 20% than other converters. PC3 is identified as an efficient voltage level converter for the LFSR counter architecture design, since it uses smaller chip area, which is approximately very lesser than the other design.

Figure 4.10 Area Analysis of level converters

The figure 4.10 illustrates the chip area analysis of the level converters (PC1, PC2 and PC3). From the graph it is clear that the level converter PC3 uses very less chip area approximately of 30 micrometer. However the simulated report may vary with that of the real time report based upon implementation. As the used chip area is
very minimum, the power dissipation by the converter is greatly reduced. The circle in the graph indicates the chip area utilization level.

4.5 SUMMARY

The proposed level converters PC1, PC2 and PC3 have no feedback path. DC current paths in CMOS gates driven by low-swing input signals, is suppressed greatly, as there is no feedback between the input and output. The less chip area usage indicates that there is very less power consumption. When the circuits are individually optimized for minimum power consumption in a 0.18-m TSMC CMOS technology, the proposed level converter PC3 offers comparatively significant power saving and improved speed.
CHAPTER 5

PERFORMANCE ANALYSIS OF CMOS VLSI

The schematic diagram of the proposed architecture is drawn and it is compiled. This level in VLSI technology is known as physical description level, and it is performed prior to implementation on the semiconductor chip. The layout diagram of the proposed architecture is obtained after the successful compilation. The synthesis report is analyzed, from which area and power consumed by the chip is found.

5.1 LAYOUT ANALYSIS OF D FLIP-FLOP DESIGN

The proposed D flip-flop design using dynamic logic is compared with the pass transistor logic, as the pass transistor has similar advantages with that of the proposed design. Based upon the synthesis report it is found that the pass transistor logic and dynamic logic are efficient. The layouts of dynamic logics and pass transistor were analyzed and it is shown in the figures 3.13 and 3.19.

The table 5.1 shows that the D-ff layout resolving the number of n-type and p-type MOS transistors to be used along with their dimensions is realized through 9 NMOS transistors and 5 PMOS transistors with corresponding channel length (L) and width (W). As the use of pass transistor reduces number of transistors required for
D flip-flop, the size of the logic device is reduced by avoiding the use of switches for supply voltages.

**Table 5.1 Details of MOS devices in design of D flip-flop using Pass transistors**

<table>
<thead>
<tr>
<th>MOS</th>
<th>W(µm)</th>
<th>L(µm)</th>
<th>W(λ)</th>
<th>L(λ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1</td>
<td>0.240</td>
<td>0.120</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>N2</td>
<td>0.240</td>
<td>0.120</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>N3</td>
<td>0.240</td>
<td>0.120</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>N4</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N5</td>
<td>0.240</td>
<td>0.120</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>N6</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N7</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N8</td>
<td>0.240</td>
<td>0.120</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>N9</td>
<td>0.900</td>
<td>0.120</td>
<td>15</td>
<td>2</td>
</tr>
<tr>
<td>P1</td>
<td>0.720</td>
<td>0.120</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>P2</td>
<td>0.720</td>
<td>0.120</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>P3</td>
<td>0.720</td>
<td>0.120</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>P4</td>
<td>0.720</td>
<td>0.120</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>P5</td>
<td>0.720</td>
<td>0.120</td>
<td>12</td>
<td>2</td>
</tr>
</tbody>
</table>
The table 5.2 determines the number of n type and p type MOS transistors to be used can be found along with their dimensions. As many applications uses D flip-flop designed using pass transistors, owing to its advantages including less number of MOS transistors, reduction in size of logic device upon elimination of supply switches, less chip area, etc.

**Table 5.2 Details of MOS devices in design of D flip-flop using Dynamic logic**

<table>
<thead>
<tr>
<th>MOS</th>
<th>W(µm)</th>
<th>L(µm)</th>
<th>W(λ)</th>
<th>L(λ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1</td>
<td>0.240</td>
<td>0.120</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>N2</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N3</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N4</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N5</td>
<td>0.900</td>
<td>0.120</td>
<td>15</td>
<td>2</td>
</tr>
<tr>
<td>P1</td>
<td>0.720</td>
<td>0.120</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>P2</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P3</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P4</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P5</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
</tbody>
</table>
Despite of so many advantages in the existing system, there is a setback in handling different logic voltage levels at each stage. For handling the voltage differences dynamic logic is preferred than the other logic, as dynamic logic requires minimum clock rate which is fast enough for the gates to perform output transitions before entering into holding state of the capacitance. The dynamic logic does not make output transition during clock cycle and it uses only the faster N transistors, there is betterment in transistor sizing optimizations. In addition, each rail can convey an arbitrary number of bits, and there are no power-wasting glitches.

5.1.1 Performance Analysis of D flip-flop design

<table>
<thead>
<tr>
<th>S.NO</th>
<th>Logic Name</th>
<th>No. of Transistors used</th>
<th>Power Consumption (µW)</th>
<th>Area (µM²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Pass transistor</td>
<td>56</td>
<td>74.82</td>
<td>465.54</td>
</tr>
<tr>
<td>2</td>
<td>Dynamic Logic</td>
<td>40</td>
<td>58.25</td>
<td>389</td>
</tr>
</tbody>
</table>
The table 5.3 illustrates the performance analysis through comparative study of D Flip-flop designed using pass transistor logic and dynamic logic. The synthesis results showed that the dynamic logic is preferred over the pass transistor logic, as the design uses less number of transistors, low power consumption and minimum chip area.

The figures 5.1, 5.2 and 5.3 exemplify the graphical representation of D flip-flop design parameter for analysis. The analysis report apparently indicates that the D flip-flop when designed using dynamic logic has maximum advantages than the other logics.

![Figure 5.1 Analysis of used number of transistors in D flip-flop design](image)

Figure 5.1 Analysis of used number of transistors in D flip-flop design
Figure 5.2 Analysis of power consumption in D flip-flop design

Figure 5.3 Analysis of area in D flip-flop design
5.1.2 LFSR counter architecture using Dynamic Logic

Several LFSR counter architecture has its D flip-flop designed using pass transistors, owing to its advantages including less number of MOS transistors, reduction in size of logic device upon elimination of supply switches, less chip area, etc. Despite of so many advantages in the existing system, there is a setback in handling different logic voltage levels at each stage. In spite of pass transistor logic dynamic logic is used as it has better performances as compared to clocked logic and various static logics. The dynamic logic requires only minimum clock rate so the output state of each dynamic gate is used before it leaks out of the capacitance holding that state. During the clock cycle the dynamic logic is not actively driven, hence it provides reliable and stable output transition. It uses only the faster N transistors, there is betterment in transistor sizing optimizations. In addition, each rail can convey an arbitrary number of bits, and there are no power-wasting glitches. The discussions showed that the Dynamic logic may be preferred to design the D flip-flop to construct a LFSR counter architecture, in view of the fact that the number MOS transistors to be used are very less. As only 5 NMOS devices and 5 PMOS devices are utilized, the total power consumed by the logic is considerably low and the chip area occupied by the device is also very minimum.
The figure 3.22 shows the schematic diagram of a LFSR counter architecture designed using dynamic logic. A synchronous clock pulse is used to provide the required clock cycles. The input bits are shifted from one flip flop to next for each clock pulse applied. The outputs, out3 and out4 are combined in exclusive-OR configuration to form a feedback mechanism and are fed back as the input to the first flip flop as shown in figure. In this design only on XOR gate is used, hence complexity is reduced efficiently.

**Table 5.4 Details of MOS devices for LFSR counter using Dynamic Logic**

<table>
<thead>
<tr>
<th>MOS</th>
<th>W (µm)</th>
<th>L (µm)</th>
<th>W</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1</td>
<td>0.240</td>
<td>0.120</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>N2</td>
<td>0.240</td>
<td>0.120</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>N3</td>
<td>0.240</td>
<td>0.120</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>N4</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N5</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N6</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N7</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N8</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N9</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N10</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N11</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N12</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N13</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N14</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>MOS</td>
<td>W (µm)</td>
<td>L (µm)</td>
<td>W</td>
<td>L</td>
</tr>
<tr>
<td>-----</td>
<td>--------</td>
<td>--------</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>N15</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N16</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N17</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N18</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N19</td>
<td>1.020</td>
<td>0.120</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>N20</td>
<td>0.240</td>
<td>0.120</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>P1</td>
<td>0.720</td>
<td>0.120</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>P2</td>
<td>0.720</td>
<td>0.120</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>P3</td>
<td>0.720</td>
<td>0.120</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>P4</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P5</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P6</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P7</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P8</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P9</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P10</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P11</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P12</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P13</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P14</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P15</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P16</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P17</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P18</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P19</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>P20</td>
<td>1.980</td>
<td>0.120</td>
<td>33</td>
<td>2</td>
</tr>
</tbody>
</table>
Figure 3.23 shows the layout diagram of LFSR counter designed using dynamic logic. Optimization of the layout is performed by checking the redundancy and floating points at the NMOS level and PMOS level. The power dissipation, delay and area analysis were made. The table 5.4 shows the detailed data sheet of all the MOS devices utilized in the design, and it is clear that the LFSR counter using dynamic logic is designed using 20 NMOS transistors and 20 PMOS transistors with specified dimensions. The report indicates that the width and length ratio of all 16 devices are identical, conversely 4 devices have different width-length ratio. The change in the ratio leads to perform scaling of devices if required.

5.1.3 Performance Analysis of LFSR architectural design

The proposed LFSR counter architecture is designed using dynamic logic. The design is synthesized and the results were analyzed. The table 5.5 illustrates the comparative study of LFSR architectural design, and it shows that the proposed design consumes minimum power when compared to the other LFSR design. The average delay of the proposed design seems to be better, as there is no unwanted metal connects between the devices. The chip area occupied by the proposed design is extremely very less when compared to the other devices.
<table>
<thead>
<tr>
<th>Name</th>
<th>Year of Publication</th>
<th>Logic Design</th>
<th>Average Delay (ns)</th>
<th>Average Power (µW)</th>
<th>Area (µm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Doshi N. A. et.al [12]</td>
<td>2008</td>
<td>NAND gates</td>
<td>-</td>
<td>106</td>
<td>-</td>
</tr>
<tr>
<td>M.Janaki Rani et.al [20]</td>
<td>2012</td>
<td>Pass Transistor</td>
<td>62</td>
<td>913</td>
<td>-</td>
</tr>
<tr>
<td>Nilesh P. Bobade et.al [47]</td>
<td>2012</td>
<td>Transmission gates</td>
<td>-</td>
<td>625</td>
<td>390.1</td>
</tr>
<tr>
<td>Nilesh P. Bobade et.al [47]</td>
<td>2012</td>
<td>Pass Transistor</td>
<td>-</td>
<td>59.22</td>
<td>460</td>
</tr>
<tr>
<td>Vikas Sahu et.al [69]</td>
<td>2013</td>
<td>Transmission Gate with Inverter</td>
<td>25</td>
<td>175</td>
<td>-</td>
</tr>
<tr>
<td>G.Ramesh et.al [50]</td>
<td>2013</td>
<td>Clocked Transmission gate</td>
<td>-</td>
<td>75</td>
<td>-</td>
</tr>
<tr>
<td>Mohd. Marufuzzaman et.al [41]</td>
<td>2014</td>
<td>NAND gates</td>
<td>-</td>
<td>683.5</td>
<td>1808.04</td>
</tr>
<tr>
<td>Proposed LFSR</td>
<td>2014</td>
<td>Dynamic Logic</td>
<td>0.0526</td>
<td>58.25</td>
<td>389</td>
</tr>
</tbody>
</table>
Figure 5.4 Comparative analysis of average power of LFSR

The figure 5.4 shows the comparative analysis of average power consumed by the LFSR design. As the newer technologies are focusing in device miniaturization and low power application, use of power for each module is now taken into account. Based upon the analysis report it is said that the average power utilized by the design is comparatively very low, as the use of dynamic logic utilizes minimum clock rate, the output state of each dynamic gate is used effectively before it leaks out as it is not actively driven. Each rail in logic conveys an arbitrary number of bits, and there are no power-wasting glitches.
Figure 5.5 Comparative analysis of average delay of LFSR

Figure 5.6 Comparative analysis of area of LFSR
The figures 5.5 and 5.6 show the graphical representation of average delay function and layout area of the LFSR design. As minimum number of transistors is used when compared to pass transistor based LFSR counter, power consumption and chip area occupied by the design will also be reduced considerably. However there will be a slight charge leakage exists in the CMOS circuits due to the unwanted conduction paths like sub threshold and reverse PN-junction currents. These drawbacks are overcome by efficient multi-threshold logic.

5.2 PERFORMANCE ANALYSIS OF LEVEL CONVERTERS

The performances of standard level converters [51, 56] were analyzed from the synthesized outputs. The table 5.6 shows the optimal power consumed by the standard level converters and proposed level converter. From the result it is clear that the both the standard converters consume more power during the low $V_{DDL}/V_{DDH}$ and it is gradually reduced upon increasing the $V_{DDL}/V_{DDH}$. The proposed level converter PC3 showed that it consumes very less power in the range of nanowatts during low $V_{DDL}/V_{DDH}$. However power consumption slight increases from nanowatts to microwatts as the multi-threshold voltage is increases. The figure 5.7 depicts the power analysis report for standard and proposed level converter. The average power of PC3 is
marked with a ring for easy representation. According to the analysis report it is comprehensible that the proposed level converter is more advantages than the other converters.

Table 5.6 Power analysis of standard and proposed level converters

<table>
<thead>
<tr>
<th>VDDL</th>
<th>VDDH</th>
<th>Name of the level converter</th>
<th>Power in µwatts</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5v</td>
<td>1.8v</td>
<td>LC1</td>
<td>9.133</td>
</tr>
<tr>
<td>0.5v</td>
<td>1.8v</td>
<td>LC2</td>
<td>7.3</td>
</tr>
<tr>
<td>0.5v</td>
<td>1.8v</td>
<td>PC3</td>
<td>0.0057</td>
</tr>
<tr>
<td>1.0v</td>
<td>1.8v</td>
<td>LC1</td>
<td>7.97</td>
</tr>
<tr>
<td>1.0v</td>
<td>1.8v</td>
<td>LC2</td>
<td>6.23</td>
</tr>
<tr>
<td>1.0v</td>
<td>1.8v</td>
<td>PC3</td>
<td>1.0485</td>
</tr>
<tr>
<td>1.2v</td>
<td>1.8v</td>
<td>LC1</td>
<td>5.97</td>
</tr>
<tr>
<td>1.2v</td>
<td>1.8v</td>
<td>LC2</td>
<td>5.82</td>
</tr>
<tr>
<td>1.2v</td>
<td>1.8v</td>
<td>PC3</td>
<td>0.7861</td>
</tr>
</tbody>
</table>
Figure 5.7 Comparative analysis of Power utilized in Level Converters

5.2.1 Synthesis results of Proposed Level Converters

Figure 5.8 Layout Simulation Result of PC1
The figures 5.8, 5.9 and 5.10 illustrate the layout of proposed multi-threshold level converters PC1, PC2 and PC3. The synthesis report indicates that the PC3 has minimum delay and utilizes minimum chip area.
Table 5.7 Optimum threshold voltages of proposed level converters

<table>
<thead>
<tr>
<th>VDDL</th>
<th>VDDH</th>
<th>Name of the level converter</th>
<th>Threshold voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5V</td>
<td>1.8V</td>
<td>PC1</td>
<td>-1.50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PC2</td>
<td>-1.44</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PC3</td>
<td>-0.56</td>
</tr>
<tr>
<td>1.0V</td>
<td>1.8V</td>
<td>PC1</td>
<td>-1.00</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PC2</td>
<td>-0.96</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PC3</td>
<td>-0.32</td>
</tr>
<tr>
<td>1.2V</td>
<td>1.8V</td>
<td>PC1</td>
<td>-0.84</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PC2</td>
<td>-0.86</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PC3</td>
<td>-0.12</td>
</tr>
</tbody>
</table>

The proposed level converters are synthesized in cadence tool and the parameters are optimized by assigning default threshold voltages. Table 5.7 illustrates the threshold voltage values for each of the converters in varies voltage ranges. Based upon the analysis results it is clear that the PC3 is more efficient compared to the PC1 and PC2.
The table 5.8 shows the power consumption and average propagation delay of the proposed level converters PC1, PC2 and PC3. From the table it is clear that the level converter PC3 consumes less power compare than PC1 and PC2.
Figure 5.11 Analysis of Average propagation delay of proposed level converters

Figure 5.11 depicts the average propagation delay of each of the level converters PC1, PC2 and PC3. It is clear that PC3 offers minimum propagation delay when optimized in various voltage levels. The figure 5.12 shows the power consumed by the converters in various $V_{DDL}$ and $V_{DDH}$ levels. It is clear from the analysis that the PC3 utilizes minimum power as compared to other converters. The low value of power indicates that it greatly reduces the total power consumption of the system when implemented.
Figure 5.12 Analysis of power consumption of proposed level converters

The figure 5.13 clearly depicts the peak power graph of each of the above mentioned level converters. It is found that the voltage level converter consumes more when the lower supply voltage $V_{DDL}$ value is very low. The power consumed by the converter gradually increases with the increase in the lower supply voltage. The $V_{DDL}$ value is increasing gradually step by step from 0.5v, 1v and 1.2v which is set as the standard voltage for the converter. The value of $V_{DDH}=1.8v$, which is a standard nominal supply voltage in CMOS technology.
Figure 5.13 Peak power graphs of the level converters

The table 5.9 exhibits the comparative analyzes of multi-threshold level converter. Based upon the analysis report it is evident that the proposed level converter has minimum propagation delay and uses very low power when compared to the other level converters.
# Table 5.9 Performance Analyzes of Multi-threshold voltage level converter

<table>
<thead>
<tr>
<th>Name</th>
<th>Year of Publication</th>
<th>Technology (nm)</th>
<th>Power (µW)</th>
<th>Average Propagation Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S.Balakrishna et.al [8]</td>
<td>2011</td>
<td>180</td>
<td>1.39</td>
<td>74.020</td>
</tr>
<tr>
<td>B.Sathyabama et.al [55]</td>
<td>2012</td>
<td>180</td>
<td>6.04</td>
<td>-----</td>
</tr>
<tr>
<td>Shanky Goyal et.al [57]</td>
<td>2013</td>
<td>45</td>
<td>38.26</td>
<td>51.580</td>
</tr>
<tr>
<td>S.Manikandan et.al [38]</td>
<td>2013</td>
<td>180</td>
<td>48.62</td>
<td>132.100</td>
</tr>
<tr>
<td>K Murali Chandra Babu et.al [43]</td>
<td>2014</td>
<td>90</td>
<td>2.137</td>
<td>101.10</td>
</tr>
<tr>
<td>S. Sinthuja et. al [60]</td>
<td>2014</td>
<td>180</td>
<td>31.0</td>
<td>-----</td>
</tr>
<tr>
<td>Proposed level converter</td>
<td>2014</td>
<td>180</td>
<td>0.005</td>
<td>0.128</td>
</tr>
</tbody>
</table>
Figure 5.14 Analysis of average propagation delay of multi-threshold voltage level converter

The figure 5.14 shows the average propagation delay of several multi-threshold voltage level converters. The proposed level converter has 0.128nsec propagation delay; hence more than 80% of delay is reduced comparative to other design.

The figure 5.15 shows the average power utilized by various multi-threshold voltage level converter design. The proposed converter is said to be superior to the other design by exhibiting maximum power consumption approximately 85%.
5.3 SUMMARY

Dynamic CMOS logic is identified as efficient, area effective and low cost design for the D flip-flop of LFSR counter, after performing complete layouts analysis. The entire LFSR architecture is designed using the efficient D flip-flop CMOS logic. High-speed and low-power multi-threshold voltage level converter for the CMOS logic is identified in order to reduce charge leakage existing in the CMOS circuit due to the unwanted conduction paths, upon optimization. The architecture with the multi-threshold level converter encompasses enhanced speed with minimum area and power consumption.
CHAPTER 6
RESULTS AND DISCUSSIONS

LFSR is used in a variety of applications including BIST, cryptography, error correction code, and in field of communication, it is much more important to implement LFSR counter architecture in hardware. In this thesis, performance evaluation of CMOS VLSI architecture of LFSR counter is analyzed. The counter design is analyzed using different technologies of CMOS; it is found that dynamic logic sounds good in all aspects including reduced propagation delay, increased speed and performance of the device. The following are the outcome of this research:

i. The D flip-flop of LFSR is designed using CMOS VLSI logics like pass transistor and dynamic CMOS logic, and layouts were analysed. The analysis results show that the dynamic logic uses only minimum number of transistors than the other logics. As dynamic logic utilizes minimum clock rate, the output state of each dynamic gate is used effectively before it leaks out as it is not actively driven. The dynamic logic uses only the faster N transistors; hence transistor sizing optimizations is done efficiently. Each rail in logic conveys an
arbitrary number of bits, and there are no power-wasting glitches.

ii. The dynamic CMOS logic is identified as an efficient for designing D flip flop, based upon the layout analysis results. The entire LFSR counter architecture is designed using the dynamic logic. The overall architecture is designed using 20 NMOS devices and 20 PMOS devices, which is far low as compared to other CMOS logics. The synthesis results show that the power utilized by the architecture is very low and average propagation delay is reduced considerably, thereby increasing the speed of the device. As minimum number of transistors is utilized, chip area occupied by this architecture is very low.

iii. High-speed and low-power multi-threshold voltage level converter is identified from three proposed level converters, based on the synthesis report. The use of this efficient multi-threshold voltage level converter at the LFSR architecture reduces charge leakage existing in the CMOS circuit due to the unwanted conduction paths.
CHAPTER 7

CONCLUSIONS

7.1 CONTRIBUTIONS

In this work, CMOS VLSI design of LFSR counter is taken for the performance evaluation. The area, time complexity and power utilization for CMOS VLSI design of proposed and existing architectures are derived and compared. The contributions that have been made to full fill the objectives of the thesis are:

i. The D flip-flop of LFSR counter which is said to be the seed is designed using pass transistor and dynamic CMOS technologies.

ii. The layout results of the D flip-flop designed using the CMOS technologies were analysed. The analysis results show that the D flip-flop developed using dynamic CMOS technology uses less number of transistors and minimum clock rate. Hence the use of this dynamic logic design reduces the chip area and power utility while enhancing the operational speed.

iii. The performance of the D flip-flop designed using dynamic logic is said to be comparatively better; therefore the entire LFSR architecture is designed using this D flip-flop.
iv. Several multi-threshold voltage level converter circuits for low and high threshold voltages were analysed.

v. Upon analysis of several level converters, the proposed level converter PC3 is identified as the efficient level converter with high processing speed and low power utilization. This level converter does not use feedback path and also suppresses dc current path driven by low voltage-swing input signals.

vi. The level converter (PC3) offers significant power saving and speed enhancement to the LFSR counter, by eliminating the static dc current and charge leakage existing in the CMOS circuits. Therefore the combination of dynamic logic with level converter (PC3) is considered as novel with reasonable area and time complexity overheads, possessing maximum efficiency and better reliability.

7.2 FUTURE WORKS

In this work, an efficient CMOS VLSI architecture for LFSR counter is proposed with performance, area and power optimization. The following are the bearing for future work.

i. The proposed architecture is designed using dynamic logic
whose performances are found better than the preceding works. The charge leakage problem is overcome by setting very high clock frequency; however this is achieved upon petite compromise in power consumption. The future work can be extended with varying clock frequencies.

ii. Future work can be extended by using combination of CMOS logics in design of master and slave D flip flop.

iii. The proposed architecture utilizes multi-threshold level converter for providing rigid voltage levels. Future work can be extended by using built-in level converter in the architecture.

iv. Future work can be extended with placement and floor-planning of level converter circuits within the architecture in an area efficient manner, in order to get miniature architectural design.
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INTERNATIONAL JOURNALS
